1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
02		384356	ENGINEERING RELEASED	06/03/05	?

BOZEMAN EVT

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	MARIAS	06/03/2005
4	4	Power Block Diagram	MARIAS	06/03/2005
5	5	Revision History	N/A	N/A
6	6	Q41C Pin Swaps	N/A	N/A
7	7	Functional Test Points	MARIAS	06/03/2005
8	8	I2C Connections	MARIAS	06/03/2005
9	9	JTAG Connections	MARIAS	06/03/2005
10	10	Power Synonyms	MARIAS	06/03/2005
11	11	Signal Synonyms	MARIAS	06/03/2005
12	12	Power Inputs	MARIAS	06/03/2005
13	13	Battery Charger	MARIAS	06/03/2005
14	14	12.8V PBUS/PMU Supplies	MARIAS	06/03/2005
15	15	5V/3.3V Supplies	MARIAS	06/03/2005
16	16	1.8V/1.5V Supplies	MARIAS	06/03/2005
17	17	2.5V Supply	MARIAS	06/03/2005
18	19	Vesta Power & Misc	MARIAS	06/03/2005
19	21	I2 Power	MARIAS	06/03/2005
20	22	I2 Power Supplies	MARIAS	06/03/2005
21	23	I2 Supplemental	MARIAS	06/03/2005
22	24	I2 Miscellaneous	MARIAS	06/03/2005
23	25	PCI Clock Buffer	MARIAS	06/03/2005
24	26	LEDs/Reset/Debug	MARIAS	06/03/2005
25	27	Power Management Unit (PMU05)	MARIAS	06/03/2005
26	29	Power Sequencing	MARIAS	06/03/2005
27	30	Fan Controller	MARIAS	06/03/2005
28	31	ALS Support	MARIAS	06/03/2005
29	32	Sudden Motion Sensor	MARIAS	06/03/2005
30	33	Q41C Internal I/O I	N/A	N/A
31	34	Q41C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	MARIAS	06/03/2005
33	36	A8 MaxBus (CPU0)	MARIAS	06/03/2005
34	37	A8 Configuration Straps	MARIAS	06/03/2005
35	38	A8 Power (CPU0)	MARIAS	06/03/2005
36	39	CPU VCore Supply	MARIAS	06/03/2005
37	46	CPU AVDD Supply	MARIAS	06/03/2005
38	47	I2 Memory Interface	MARIAS	06/03/2005
39	48	Memory Series Termination	MARIAS-NDIFF	N/A
40	50	DDR2 SO-DIMM Slot A	MARIAS-MDIFF	N/A
41	52	DDR2 SO-DIMM Slot B	MARIAS-MDIFF	N/A
42	55	M11 Frame Buffer Constraints	MARIAS	06/03/2005
43	56	I2 AGP Interface	MARIAS	06/03/2005
44	57	GPU (M11) AGP Interface	MARIAS	06/03/2005
45	58	GPU VCore Supply	MARIAS	06/03/2005
46	59	GPU (M11) Core Power	MARIAS	06/03/2005
47	60	GPU (M11) I/O Power	MARIAS	06/03/2005
48	61	GPU (M11) Frame Buffer I/F	MARIAS	06/03/2005
49	62	GPU Frame Buffer A	MARIAS	06/03/2005
50	63	GPU Frame Buffer B	MARIAS	06/03/2005
51	64	GPU (M11) GPIOs/Straps	MARIAS	06/03/2005
52	65	GPU (M11) Clocks/Misc	MARIAS	06/03/2005
53	66	GPU (M11) DVI/DAC Outputs	MARIAS	06/03/2005
54	67	Lower TMDS Transmitter	MARIAS	06/03/2005
55	68	Upper TMDS Transmitter	MARIAS	06/03/2005
56	69	Internal Display Conns	MARIAS	06/03/2005
57	70	External Display Conns	MARIAS-PDIFF	06/02/2005
58	71	BootROM	MARIAS	06/03/2005
59	72	I2 PCI Interface	MARIAS	06/03/2005
60	73	Q85 AIRPORT/BT CONN	MARIAS-MDIFF	N/A
61	74	Cardbus	MARIAS	06/03/2005
62	75	NEC USB2	MARIAS	06/03/2005
63	81	I2 UATA Interface	MARIAS	06/03/2005
64	82	HDD/ODD Connectors	MARIAS-PDIFF	06/02/2005
65	84	I2 Ethernet Interface	MARIAS	06/03/2005
66	85	Vesta Ethernet PHY	MARIAS	06/03/2005
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	MARIAS	06/03/2005
69	89	Vesta FireWire PHY	MARIAS	06/03/2005
70	90	FireWire Ports	MARIAS-PDIFF	06/02/2005
71	91	FireWire Series Term	MARIAS	06/03/2005
72	92	I2 USB Interface	MARIAS	06/03/2005
73	93	NEC USB2 Interface	MARIAS	06/03/2005
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	MARIAS	06/03/2005
76	111	Spacing & Physical Constraints 2	MARIAS	06/03/2005
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6839	1	SCHEM,BOZEMAN,Q41C	SCH1	
820-1810	1	PCBF,BOZEMAN,Q41C	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYV]	VRAM_SAMSUNG
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TML]	VRAM_HYNIX

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±

DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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TITLE
SCHEM,BOZEMAN,Q41C

DRAWING NUMBER 051-6839 REV. 02

Design-Specific Rules

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
    STANDARD    =DEFAULT    *    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_SPACING_RULE
    BGA_P1MM    10    *    0.10 MM    1.25 MM    0.1 MM    12.5 MM    15.0 MM
TABLE_SPACING_RULE
    BGA_P2MM    20    *    0.20 MM    1.25 MM    0.1 MM    12.5 MM    15.0 MM
TABLE_SPACING_RULE
    DEFAULT    *    0.1 MM    2.5 MM    0.15 MM    10.0 MM    15.0 MM
TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT
    *    *    1MM    BGA_P1MM
TABLE_SPACING_ASSIGNMENT
    AGP_STB    *    1MM    BGA_P2MM
TABLE_SPACING_ASSIGNMENT
    CLOCK    *    1MM    BGA_P2MM
TABLE_SPACING_ASSIGNMENT
    RAM_DIFF    *    1MM    BGA_P2MM
```

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.

"BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

```
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    STANDARD    *    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_PHYSICAL_RULE
    DEFAULT    *    Y    0.100 MM    0.100 mm    1.25 MM
```

Layer-specific rules for 90-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    90_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.200 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    90_OHM_DIFF    *    2.5 MM    0.200 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    90_OHM_DIFF    TOP,BOTTOM    Y    0.118 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    90_OHM_DIFF    *    Y    0.125 MM    0.1 MM    5 MM
```

Layer-specific rules for 100-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    100_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.200 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    100_OHM_DIFF    *    2.5 MM    0.200 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    100_OHM_DIFF    TOP,BOTTOM    Y    0.092 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    100_OHM_DIFF    *    Y    0.100 MM    0.1 MM    5 MM
```

Layer-specific rules for 110-ohm differential impedance

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    110_OHM_DIFF    TOP,BOTTOM    2.5 MM    0.330 MM    2.5 MM    1.0 MM
TABLE_SPACING_RULE
    110_OHM_DIFF    *    2.5 MM    0.300 MM    2.5 MM    1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    110_OHM_DIFF    TOP,BOTTOM    Y    0.080 MM    0.1 MM    5 MM
TABLE_PHYSICAL_RULE
    110_OHM_DIFF    *    Y    0.085 MM    0.1 MM    5 MM
```

Portable-specific Override Rules

```
TABLE_SPACING_RULE

TABLE_SPACING_RULE
    AGP    201    *    0.2 MM
TABLE_SPACING_RULE
    AGP_STB    251    *    0.25 MM
TABLE_SPACING_RULE
    VGA    151    *    0.15 MM    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT
TABLE_SPACING_RULE
    TV    151    *    0.15 MM    =DEFAULT    =DEFAULT    =DEFAULT    =DEFAULT

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    VGA    *    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE
TABLE_PHYSICAL_RULE
    TV    *    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE    =60_OHM_SE
```

CHASSIS GND CONNECTIONS

Layer-specific rules for 60-ohm single-ended impedance

```
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    60_OHM_SE    *    Y    0.076 MM    =50_OHM_SE    =50_OHM_SE
```

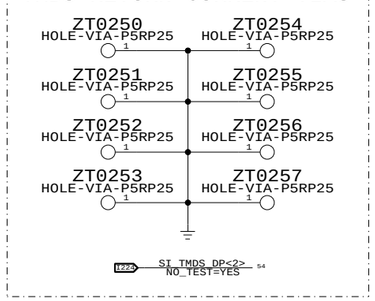
Layer-specific rules for 50-ohm single-ended impedance

```
TABLE_SPACING_RULE

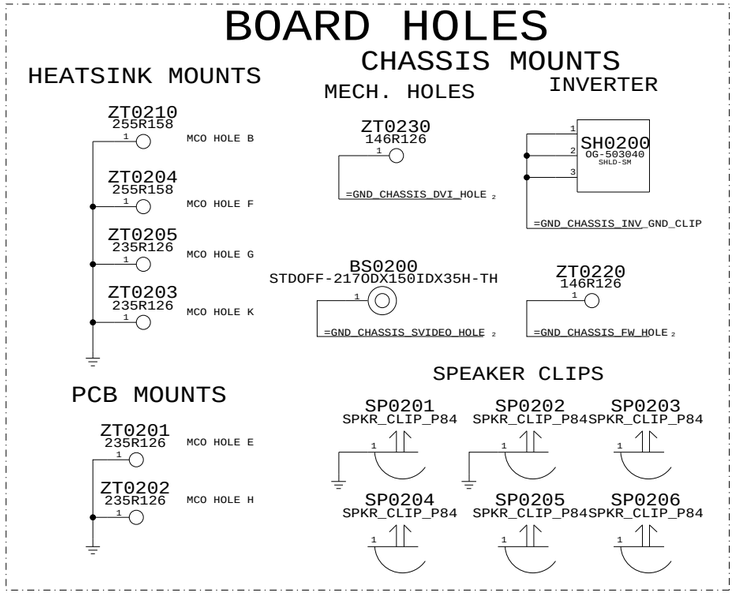
TABLE_SPACING_RULE
    50_OHM_SE    *    2.5 MM    0.125 MM    2.5 MM    1.0 MM
TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE
    50_OHM_SE    *    Y    0.100 MM    0.100 MM    1.25 MM
```

TMDS RETURN CURRENT VIAS



BOARD HOLES



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA

1		SIGNAL (1/2 OZ + COPPER PLATING)
2	PREPREG	GROUND (1/2 OZ)
3	CORE	SIGNAL (1/2 OZ)
4	PREPREG	SIGNAL (1/2 OZ)
5	CORE	GROUND (1/2 OZ)
6	PREPREG	CUT POWER PLANE (1 OZ)
7	CORE	CUT POWER PLANE (1 OZ)
8	PREPREG	GROUND (1/2 OZ)
9	CORE	SIGNAL (1/2 OZ)
10	PREPREG	SIGNAL (1/2 OZ)
11	CORE	GROUND (1/2 OZ)
12	PREPREG	SIGNAL (1/2 OZ + COPPER PLATING)

```
TABLE_BOARD_INFO
    TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM    NO_TYPE,1MM    MM
```

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7017	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_S,Q41C	COMMON,ALTERNATE,VRAM_SAMSUNG,gQ41C,gCommon
630-7186	PCBA,MLB,BESTMHZ,BOZEMAN,VRAM_H,Q41C	COMMON,ALTERNATE,VRAM_HYNIX,gQ41C,gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC,BACKUP_BATT,CPU_A7PM,I2_FW_BETA,I2_MAXBUS_50OHM,MAXBUS_1V8,gCommon1
gCommon1	MMM_ACCEL_KIONIX,GPU_PWRPLAY,GPU_SS,GPU_LVDDR_2V8,GPU_MEMIO_1V8,gCommon2
gCommon2	I2_REV1_NOT,I2_MAXBUS_FBCLK_MATCHED,I2_AGP_FBCLK_MATCHED,I2_PCI_FBCLK_MATCHED,gCommon3
gCommon3	CPU_VCORE_3STATES,I2_MAXBUS_166MHZ,CPU0_BUSRATIO_10.0X,I2VCORE_1V5,I2VCORE_BURST,gCommon4
gCommon4	VESTA_PORT2_DISABLE,DVO_1V8,TMDS_DUAL,VCORE_OFFSET,VCORE_OFFSET_SW,gUSB
gUSB	USB2_NEC,USB1P1_I2
gQ41C	Q41C_PARTS,A7PM_1P67_LGA,BOOTROM_PROG,PMU_PROG,DEVELOPMENT,MAXBUS_TBEN_SYNC

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0325	1	IC,ASIC,I2,REV1.1,NB/SB,974 BGA	U2100	CRITICAL	
337S3135	1	IC,PMU05,BLANK,QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC,PMU05,Vxxx,QFP	U2700	CRITICAL	PMU_PROG
337S3181	1	IC,A7PM,R1.5,1.67GHZ,LGA,1.28V,25W,85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3077	1	IC,A8,xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC,GPU,M11P	U5700	CRITICAL	
335S0088	1	BOOTROM,BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1739	1	IC,BOOTROM,B,Q41C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U8500	CRITICAL	
333S0317	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_HYNIX

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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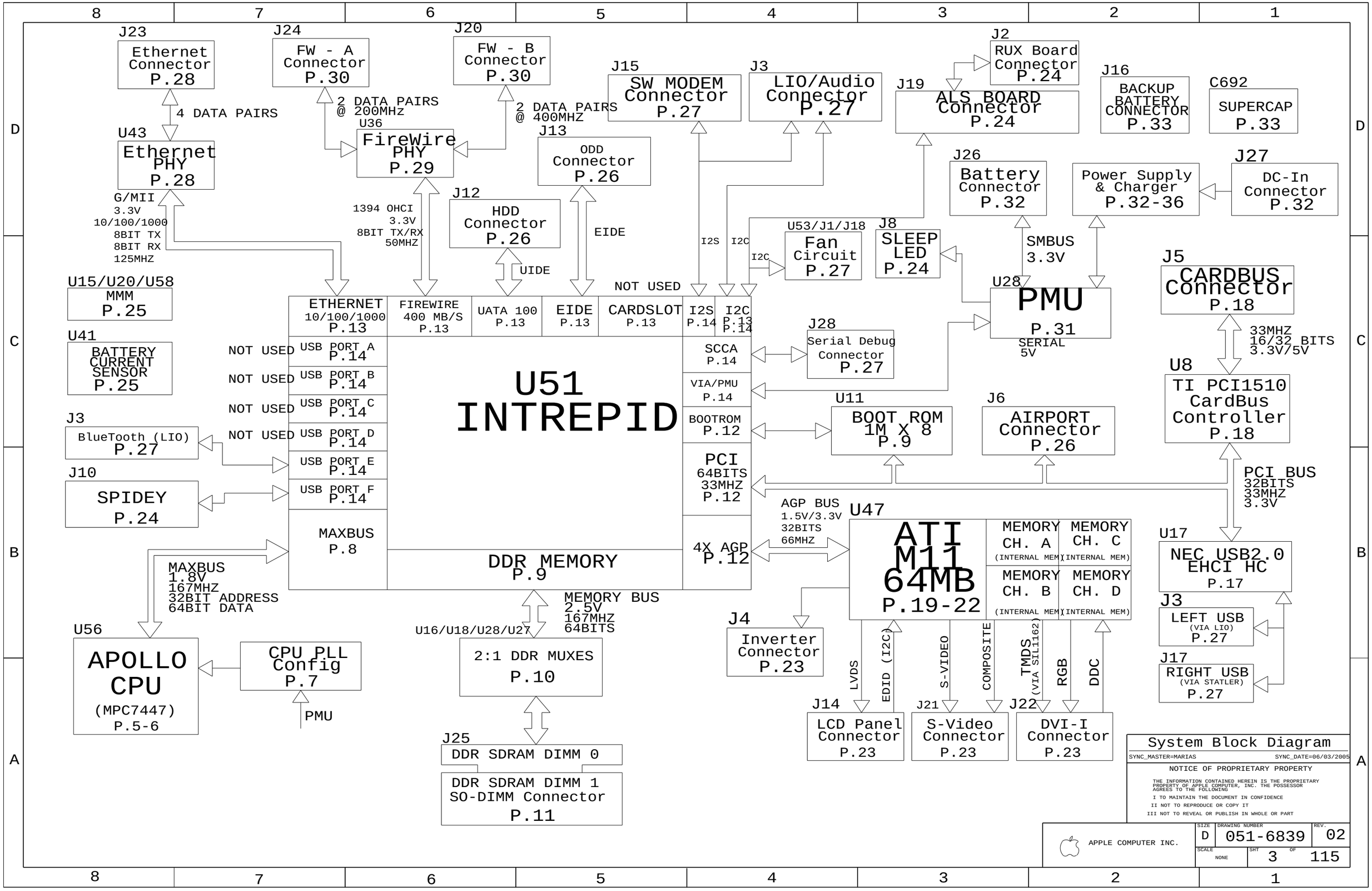
J23
Ethernet Connector P.28
J24
FW - A Connector P.30
J20
FW - B Connector P.30
J15
SW MODEM Connector P.27
J3
LIO/Audio Connector P.27
J2
RUX Board Connector P.24
J19
ALS BOARD Connector P.24
J16
BACKUP BATTERY CONNECTOR P.33
C692
SUPERCAP P.33
4 DATA PAIRS
2 DATA PAIRS @ 200MHz
2 DATA PAIRS @ 400MHZ
U36
FireWire PHY P.29
J13
ODD Connector P.26
U43
Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
1394 OHCI
3.3V
8BIT TX/RX
50MHZ
J12
HDD Connector P.26
EIDE
UIDE
J26
Battery Connector P.32
Power Supply & Charger P.32-36
J27
DC-In Connector P.32
U53/J1/J18
Fan Circuit P.27
J8
SLEEP LED P.24
I2S
I2C
SMBUS
3.3V
U15/U20/U58
MMM P.25
NOT USED
ETHERNET 10/100/1000 P.13
FIREWIRE 400 MB/S P.13
UATA 100 P.13
EIDE P.13
CARDSLOT P.13
I2S P.14
I2C P.13 P.14
U28
PMU P.31
SERIAL
5V
J5
CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U41
BATTERY CURRENT SENSOR P.25
NOT USED
USB PORT A P.14
USB PORT B P.14
USB PORT C P.14
USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
U51
INTREPID
SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12
J28
Serial Debug Connector P.27
U8
TI PCI1510 CardBus Controller P.18
U11
BOOT ROM 1M X 8 P.9
J6
AIRPORT Connector P.26
J3
BlueTooth (LIO) P.27
J10
SPIDEY P.24
MAXBUS P.8
DDR MEMORY P.9
PCI BUS
32BITS
33MHZ
3.3V
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47
ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
U17
NEC USB2.0 EHCI HC P.17
MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27
2:1 DDR MUXES P.10
J4
Inverter Connector P.23
J3
LEFT USB (VIA LIO) P.27
J17
RIGHT USB (VIA STATLER) P.27
U56
APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
J14
LCD Panel Connector P.23
J21
S-Video Connector P.23
J22
DVI-I Connector P.23
J25
DDR SDRAM DIMM 0
DDR SDRAM DIMM 1
SO-DIMM Connector P.11
System Block Diagram
SYNC_MASTER=MARIAS
SYNC_DATE=06/03/2005
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REV. 02
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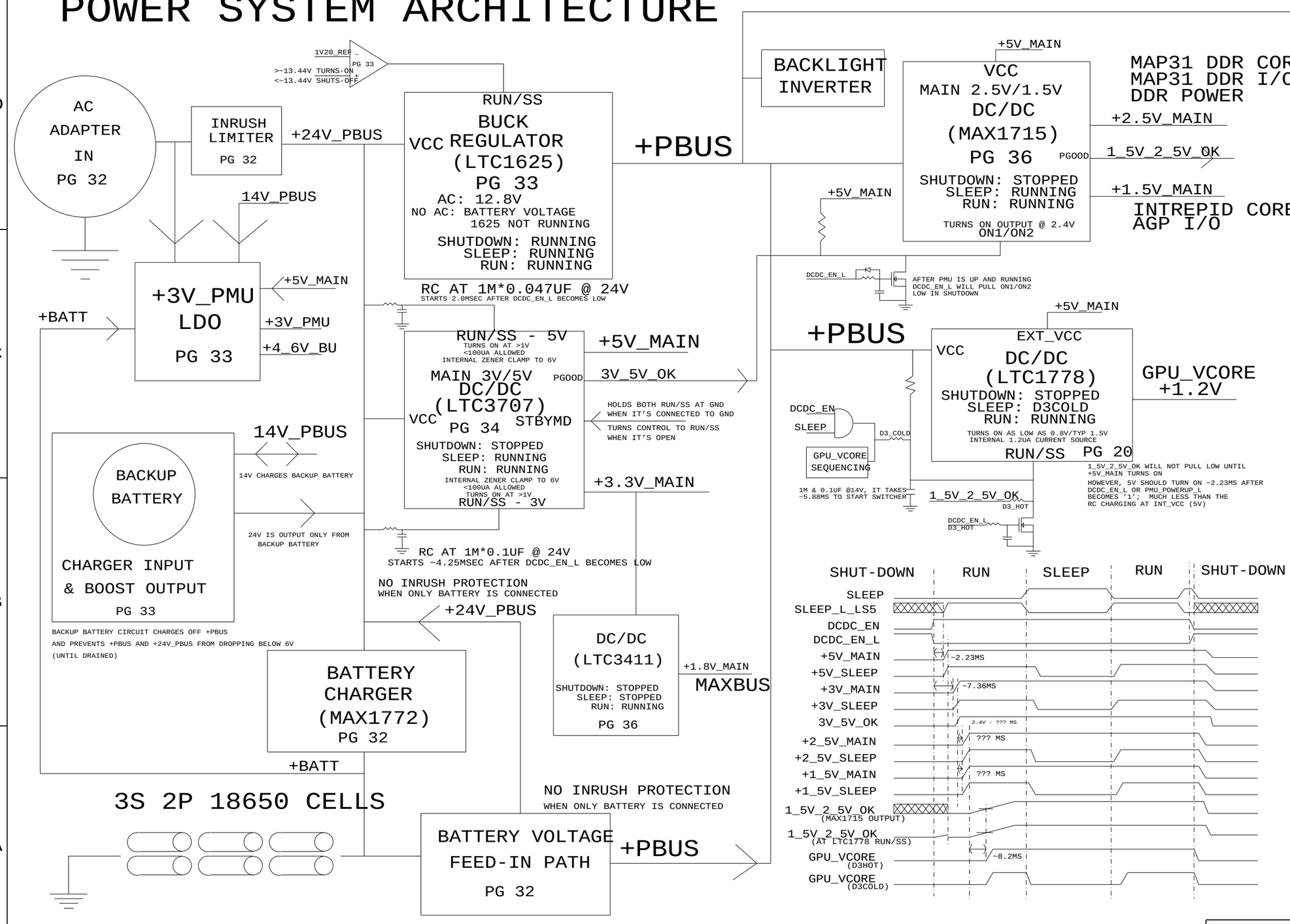
SHT 3 OF 115

POWER SYSTEM ARCHITECTURE



Power Block Diagram

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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REVISION HISTORY

PROTO

```
04/05/2005 - Beginning revision history
           - Sync'd FB pin swaps from 051-5838
           - Pinned out audio connector per flex cable
           - Pinned out left USB/ALS connector per flex cable
04/07/2005 - Moved modem connector to non-shared page
           - Updated chassis ground connections
           - Pin swapped DDR2 according to layout
04/11/2005 - Changed audio caps to X5R (CA033, CA050, CA051)
04/12/2005 - Updated wireless connector pinout according to flex
           - Implemented more DDR2 pin swaps
           - Implemented pin swaps on FW data lines
           - Added RAM DQS_N pulldowns
           - Corrected mdsr line and neck width properties
04/14/2005 - Switched GPU to M11
04/15/2005 - Added CPU Vcore mux circuit
04/19/2005 - Added NO_TEST property to buses between JTAG enabled devices
           - Pinswapped FB V7 for M11
04/20/2005 - Corrected ENET power rail to PWRON instead of RUN (Wake-on-LAN)
           - Corrected Vesta reset and ethernet LOWPWR circuits
           - Changed Rs480 to 6.34k to take GPU Vcore to 1.3V/1.05V
           - Added page 6 and modified pages 11,35,61 for design specific pin swaps
           - Separated GPU MVREF into two dividers
04/26/2005 - Added 8 vias for TMDS return current
           - Added LVDS electrical constraint set properties
04/27/2005 - Added NO_ECL_PROPERTY to SI_TMDS_DEC_PCB (no room for TP)
           - Changed MIN_NECK_WIDTH property on TMDS power rails to 0.2 mm
           - Changed gender of debug connector
           - Removed C6367 due to MC0 violation
04/29/2005 - Schematic released as REV 01 for PROTO
```

EVT

```
05/04/2005 - Added SYNONYMS to allow DVO and USB pulldown pinswaps
05/09/2005 - Added missing pullup to SYS_LID_OPEN
           - Added missing pulldown to Vesta LPWR 1394
05/09/2005 - Lead-free resistor replacement on page 86
05/16/2005 - Various lead-free replacements
           - Added Hynix VRAM option and PCBA
05/17/2005 - Added 2 0.1uF caps to VGA sync buffers
05/25/2005 - Added NEC USB2 controller and pci clock buffer
           - Various lead-free replacements
           - Added pullup to BATT0_DET
05/26/2005 - Removed SMS PIC microcontroller
05/31/2005 - Added 2 0.1uF caps to GPU Vcore output
           - Corrected USB diff pair and spacing/physical rules on ports
06/01/2005 - Corrected caps on Firewire V8 rail to 50V
           - Various lead-free replacements
```

02

SYNC_MASTER=N/A SYNC_DATE=N/A

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SCALE NONE	SHT 5 OF 115	

I2S Series Rs

MAKE_BASE=TRUE	22	I2S0_SB_TO_DEV_DTO_R	=RP1150P1	11	11	=RP1150P8	I2S0_SB_TO_DEV_DTO	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_BITCLK_R	=RP1150P2	11	11	=RP1150P7	I2S0_BITCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_MCLK_R	=RP1150P3	11	11	=RP1150P6	I2S0_MCLK	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S0_SYNC_R	=RP1150P4	11	11	=RP1150P5	I2S0_SYNC	7 74	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SB_TO_DEV_DTO_R	=RP1151P1	11	11	=RP1151P8	I2S1_SB_TO_DEV_DTO	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_SYNC_R	=RP1151P2	11	11	=RP1151P7	I2S1_SYNC	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_MCLK_R	=RP1151P3	11	11	=RP1151P6	I2S1_MCLK	30	MAKE_BASE=TRUE
MAKE_BASE=TRUE	22	I2S1_BITCLK_R	=RP1151P4	11	11	=RP1151P5	I2S1_BITCLK	30	MAKE_BASE=TRUE

UATA Series Rs

MAKE_BASE=TRUE	63	UATA_DD_R<12>	=RP8150P1	63	63	=RP8150P8	UATA_DD<12>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_CS0_L_R	=RP8150P2	63	63	=RP8150P7	UATA_CS0_L	7 63 64	MAKE_BASE=TRUE (IDE_CS1FX_L)
MAKE_BASE=TRUE	63	UATA_DD_R<14>	=RP8150P3	63	63	=RP8150P6	UATA_DD<14>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<11>	=RP8150P4	63	63	=RP8150P5	UATA_DD<11>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<7>	=RP8151P1	63	63	=RP8151P8	UATA_DD<7>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<2>	=RP8151P2	63	63	=RP8151P7	UATA_DD<2>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<3>	=RP8151P3	63	63	=RP8151P6	UATA_DD<3>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<15>	=RP8151P4	63	63	=RP8151P5	UATA_DD<15>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<9>	=RP8152P1	63	63	=RP8152P8	UATA_DD<9>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<4>	=RP8152P2	63	63	=RP8152P7	UATA_DD<4>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<6>	=RP8152P3	63	63	=RP8152P6	UATA_DD<6>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<5>	=RP8152P4	63	63	=RP8152P5	UATA_DD<5>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<2>	=RP8153P1	63	63	=RP8153P8	UATA_DA<2>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<8>	=RP8153P2	63	63	=RP8153P7	UATA_DD<8>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<10>	=RP8153P3	63	63	=RP8153P6	UATA_DD<10>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<0>	=RP8153P4	63	63	=RP8153P5	UATA_DA<0>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<13>	=RP8154P1	63	63	=RP8154P8	UATA_DD<13>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<0>	=RP8154P2	63	63	=RP8154P7	UATA_DD<0>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DD_R<1>	=RP8154P3	63	63	=RP8154P6	UATA_DD<1>	7 63 64	MAKE_BASE=TRUE
MAKE_BASE=TRUE	63	UATA_DA_R<1>	=RP8154P4	63	63	=RP8154P5	UATA_DA<1>	7 63 64	MAKE_BASE=TRUE

Lower DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<0>	=RP6720P1	54	54	=RP6720P8	GPU_DVOD<0>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<1>	=RP6720P2	54	54	=RP6720P7	GPU_DVOD<1>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<2>	=RP6720P3	54	54	=RP6720P6	GPU_DVOD<2>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<3>	=RP6720P4	54	54	=RP6720P5	GPU_DVOD<3>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<11>	=RP6721P1	54	54	=RP6721P8	GPU_DVOD<11>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<10>	=RP6721P2	54	54	=RP6721P7	GPU_DVOD<10>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<9>	=RP6721P3	54	54	=RP6721P6	GPU_DVOD<9>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<8>	=RP6721P4	54	54	=RP6721P5	GPU_DVOD<8>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<6>	=RP6722P1	54	54	=RP6722P8	GPU_DVOD<6>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<4>	=RP6722P2	54	54	=RP6722P7	GPU_DVOD<4>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<7>	=RP6722P3	54	54	=RP6722P6	GPU_DVOD<7>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<5>	=RP6722P4	54	54	=RP6722P5	GPU_DVOD<5>	54	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_HSYNC_R	=RP6723P1	54	54	=RP6723P8	GPU_DVO_HSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_VSYNC_R	=RP6723P2	54	54	=RP6723P7	GPU_DVO_VSYNC	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_DE_R	=RP6723P3	54	54	=RP6723P6	GPU_DVO_DE	54 55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVO_CLKP_R	=RP6723P4	54	54	=RP6723P5	GPU_DVO_CLKP	54 55	MAKE_BASE=TRUE

Upper DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<13>	=RP6821P1	55	55	=RP6821P8	GPU_DVOD<13>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<12>	=RP6821P2	55	55	=RP6821P7	GPU_DVOD<12>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<14>	=RP6821P3	55	55	=RP6821P6	GPU_DVOD<14>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<15>	=RP6821P4	55	55	=RP6821P5	GPU_DVOD<15>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<18>	=RP6822P1	55	55	=RP6822P8	GPU_DVOD<18>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<19>	=RP6822P2	55	55	=RP6822P7	GPU_DVOD<19>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<16>	=RP6822P3	55	55	=RP6822P6	GPU_DVOD<16>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<17>	=RP6822P4	55	55	=RP6822P5	GPU_DVOD<17>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<21>	=RP6823P1	55	55	=RP6823P8	GPU_DVOD<21>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<20>	=RP6823P2	55	55	=RP6823P7	GPU_DVOD<20>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<23>	=RP6823P3	55	55	=RP6823P6	GPU_DVOD<23>	55	MAKE_BASE=TRUE
MAKE_BASE=TRUE	53	GPU_DVOD_R<22>	=RP6823P4	55	55	=RP6823P5	GPU_DVOD<22>	55	MAKE_BASE=TRUE

MAXBUS Pullups

MAKE_BASE=TRUE	33 32	MAXBUS_TS_L	=RP3510P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BG_L	=RP3510P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DBG_L	=RP3510P3	32
MAKE_BASE=TRUE	32	MAXBUS_TBEN_I2	=RP3510P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BG_L	=RP3511P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_HIT_L	=RP3511P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_HIT_L	=RP3511P3	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BR_L	=RP3511P4	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BR_L	=RP3512P1	32
MAKE_BASE=TRUE	33 32	MAXBUS_TA_L	=RP3512P2	32
MAKE_BASE=TRUE	34 32	MAXBUS_CPU0_INT_L	=RP3512P3	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_INT_L	=RP3512P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DRDY_L	=RP3513P2	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DRDY_L	=RP3513P3	32
MAKE_BASE=TRUE	33 32	MAXBUS_AACK_L	=RP3513P4	32
MAKE_BASE=TRUE	33 32	MAXBUS_ARTRY_L	=RP3514P1	32
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DBG_L	=RP3514P2	32
MAKE_BASE=TRUE	33 32	MAXBUS_TEA_L	=RP3514P3	32

AGP Pullups

MAKE_BASE=TRUE	44 43	AGP_TRDY_L	=RP5610P1	43
MAKE_BASE=TRUE	44 43	AGP_IRDY_L	=RP5610P2	43
MAKE_BASE=TRUE	44 43	AGP_REQ_L	=RP5610P3	43
MAKE_BASE=TRUE	44 43	AGP_RBF_L	=RP5610P4	43
MAKE_BASE=TRUE	44 43	AGP_FRAME_L	=RP5611P1	43
MAKE_BASE=TRUE	44 43	AGP_DEVSEL_L	=RP5611P2	43
MAKE_BASE=TRUE	44 43	AGP_STOP_L	=RP5611P3	43
MAKE_BASE=TRUE	44 43	AGP_GNT_L	=RP5611P4	43

PCI Pullups

MAKE_BASE=TRUE	11	PCI_AIRPORT_GNT_L	=RP7250P1	59
MAKE_BASE=TRUE	60 59 62 61	PCI_TRDY_L	=RP7250P2	59
MAKE_BASE=TRUE	60 59 62 61	PCI_IRDY_L	=RP7250P3	59
MAKE_BASE=TRUE	60 59 62 61	PCI_STOP_L	=RP7250P4	59
MAKE_BASE=TRUE	11	PCI_CBUS_REQ_L	=RP7251P1	59
MAKE_BASE=TRUE	11	PCI_AIRPORT_REQ_L	=RP7251P2	59
MAKE_BASE=TRUE	11	PCI_CBUS_GNT_L	=RP7251P3	59
MAKE_BASE=TRUE	60 59 62 61	PCI_FRAME_L	=RP7251P4	59

USB Pulldowns

72	=RP9210P8	USB2_I2_LEFT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9210P7	USB2_I2_LEFT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9210P6	USB2_I2_P<1>	72	MAKE_BASE=TRUE
72	=RP9210P5	USB2_I2_N<1>	72	MAKE_BASE=TRUE
72	=RP9211P8	USB2_I2_RIGHT_PORT_P	11	MAKE_BASE=TRUE
72	=RP9211P7	USB2_I2_RIGHT_PORT_N	11	MAKE_BASE=TRUE
72	=RP9211P6	USB2_I2_P<3>	72	MAKE_BASE=TRUE
72	=RP9211P5	USB2_I2_N<3>	72	MAKE_BASE=TRUE
72	=RP9212P8	USB_I2_BT_P	11	MAKE_BASE=TRUE
72	=RP9212P7	USB_I2_BT_N	11	MAKE_BASE=TRUE
72	=RP9212P6	USB_I2_TPAD_P	11	MAKE_BASE=TRUE
72	=RP9212P5	USB_I2_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9300P8	USB2_NEC_LEFT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9300P7	USB2_NEC_LEFT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P6	USB2_NEC_RIGHT_PORT_N	11	MAKE_BASE=TRUE
73	=RP9300P5	USB2_NEC_RIGHT_PORT_P	11	MAKE_BASE=TRUE
73	=RP9301P8	USB_NEC_BT_P	11	MAKE_BASE=TRUE
73	=RP9301P7	USB_NEC_BT_N	11	MAKE_BASE=TRUE
73	=RP9301P6	USB_NEC_TPAD_N	11	MAKE_BASE=TRUE
73	=RP9301P5	USB_NEC_TPAD_P	11	MAKE_BASE=TRUE

FW Series Rs

MAKE_BASE=TRUE	68 9	FW_D_R<3>	=RP9100P1	71	71	=RP9100P8	FW_D<3>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<1>	=RP9100P2	71	71	=RP9100P7	FW_D<1>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<0>	=RP9100P3	71	71	=RP9100P6	FW_D<0>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<2>	=RP9100P4	71	71	=RP9100P5	FW_D<2>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<7>	=RP9101P1	71	71	=RP9101P8	FW_D<7>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<5>	=RP9101P2	71	71	=RP9101P7	FW_D<5>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<6>	=RP9101P3	71	71	=RP9101P6	FW_D<6>	9 69	MAKE_BASE=TRUE
MAKE_BASE=TRUE	68 9	FW_D_R<4>	=RP9101P4	71	71	=RP9101P5	FW_D<4>	9 69	MAKE_BASE=TRUE

Q41C Pin Swaps

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6839 | REV. 02
SCALE NONE | SHT 6 OF 115

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

POWER	TP12	PP24V_ADAPTER	10	FUNC_TEST=YES
	TP1	PP24V_ALL_PBUSA	10	FUNC_TEST=YES
	TP2	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES
	TP4	PPVCORE_RUN_GPU	10	FUNC_TEST=YES
	TP3	PPVCORE_RUN_CPU	10	FUNC_TEST=YES
	TP6	PP1V8_PWRON	10	FUNC_TEST=YES
	TP5	PP2V5_PWRON	10	FUNC_TEST=YES
	TP7	PP5V_PWRON	10	FUNC_TEST=YES
	TP8	PP3V3_PWRON	10	FUNC_TEST=YES
	TP9	PP5V_RUN	10	FUNC_TEST=YES
	TP10	PP3V3_ALL	10	FUNC_TEST=YES
	TP62	=FTP_GND	7 10	FUNC_TEST=YES

Place 2 TPs @ connector

Place within 50 mm of power supply.

Place 5-10 GND TPs.

LVDS	TP79	LVDS_U0_P	53 56	FUNC_TEST=YES
	TP80	LVDS_U0_N	53 56	FUNC_TEST=YES
	TP81	LVDS_U1_P	53 56	FUNC_TEST=YES
	TP82	LVDS_U1_N	53 56	FUNC_TEST=YES
	TP83	LVDS_U2_P	53 56	FUNC_TEST=YES
	TP84	LVDS_U2_N	53 56	FUNC_TEST=YES
	TP85	CLKLVDS_U_P	53 56	FUNC_TEST=YES
	TP86	CLKLVDS_U_N	53 56	FUNC_TEST=YES
	TP11	LVDS_L0_P	53 56	FUNC_TEST=YES
	TP12	LVDS_L0_N	53 56	FUNC_TEST=YES
	TP13	LVDS_L1_P	53 56	FUNC_TEST=YES
	TP14	LVDS_L1_N	53 56	FUNC_TEST=YES
	TP16	LVDS_L2_P	53 56	FUNC_TEST=YES
	TP15	LVDS_L2_N	53 56	FUNC_TEST=YES
	TP17	CLKLVDS_L_P	53 56	FUNC_TEST=YES
	TP18	CLKLVDS_L_N	53 56	FUNC_TEST=YES
	TP19	LVDS_DDC_CLK	51 56	FUNC_TEST=YES
	TP20	LVDS_DDC_DATA	51 56	FUNC_TEST=YES
	TP21	=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES
	TP63	PP3V3_LCD_CONN	56	FUNC_TEST=YES

Place within 25 mm of LVDS connector.

INVERTER	TP22	PPBUS_INVERTER	56	FUNC_TEST=YES
	TP23	PP5V_INV_SW	56	FUNC_TEST=YES
	TP25	BRIGHT_PWM	56	FUNC_TEST=YES
	TP24	GND_INVERTER	56	FUNC_TEST=YES

Place within 25 mm of inverter connector.

UATA	TP106	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES
	TP117	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES
	TP118	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES
	TP32	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES
	TP33	UATA_DMARQ	63 64	FUNC_TEST=YES
	TP35	UATA_DSTROBE	63 64	FUNC_TEST=YES
	TP34	UATA_DMACK_L	63 64	FUNC_TEST=YES
	TP36	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES
	TP38	UATA_CS0_L	6 63 64	FUNC_TEST=YES
	TP37	UATA_CS1_L	63 64	FUNC_TEST=YES
	TP40	UATA_RESET_L	63 64	FUNC_TEST=YES
	TP39	UATA_HSTROBE	63 64	FUNC_TEST=YES
	TP41	UATA_STOP	63 64	FUNC_TEST=YES
	TP42	UATA_INTRQ	63 64	FUNC_TEST=YES

Place within 50 mm of ODD/HDD connector.

AUDIO	TP76	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES
	TP60	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES
	TP59	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES
	TP61	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES
	TP44	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES
	TP46	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES
	TP48	I2S0_MCLK	6 74	FUNC_TEST=YES
	TP47	I2S0_BITCLK	6 74	FUNC_TEST=YES
	TP50	I2S0_SYNC	6 74	FUNC_TEST=YES
	TP49	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES
	TP51	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES
	TP53	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES
	TP52	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES
	TP56	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES
	TP55	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES
	TP57	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES
	TP58	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES
	TP107	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES
	TP108	AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES
	TP109	AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES
	TP110	AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES
	TP111	AUDIO_GPIO_11	22 74	FUNC_TEST=YES
	TP112	GND_AUDIO_AGND	74	FUNC_TEST=YES
	TP113	GND_AUDIO_PGND	74	FUNC_TEST=YES

Place within 25 mm of audio connector.

SYSTEM	TP76	PP5V_TPAD_F	30	FUNC_TEST=YES
	TP77	USB_TPAD_P	11 30	FUNC_TEST=YES
	TP78	USB_TPAD_N	11 30	FUNC_TEST=YES
	TP88	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES
	TP89	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES
	TP43	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES
	TP45	SYS_LID_OPEN_F	30	FUNC_TEST=YES
	TP30	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES
	TP29	=FTP_SLEEP_LED	74	FUNC_TEST=YES
	TP31	SYS_CHARGE_LED_L	24 31	FUNC_TEST=YES
	TP87	SYS_ADAPTER_ANALOG_AC_DET	12 31	FUNC_TEST=YES
	TP90	KBDLED_ANODE	28 30	FUNC_TEST=YES
	TP91	KBDLED_RETURN	28 30	FUNC_TEST=YES
	TP105	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES
	TP104	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES

Place within 25 mm of TPAD connector.

CPU FAN	TP100	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES
	TP98	FAN1_TACH	27 31	FUNC_TEST=YES
	TP97	FAN1_PWM	27 31	FUNC_TEST=YES
	TP119	=FTP_GND	7 10	FUNC_TEST=YES

Place within 25 mm of fan connector.

GPU FAN	TP102	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES
	TP103	FAN2_TACH	27 31	FUNC_TEST=YES
	TP101	FAN2_PWM	27 31	FUNC_TEST=YES
	TP120	=FTP_GND	7 10	FUNC_TEST=YES

Place within 25 mm of fan connector.

ALS	TP70	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES
	TP68	ALS_0_OUT	25 31	FUNC_TEST=YES
	TP69	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES

Place within 25 mm of ALS connector.

SCCA	TP72	SCCA_RXD	22 24	FUNC_TEST=YES
	TP71	SCCA_TXD_L	22 24	FUNC_TEST=YES

Place within 25 mm of debug connector.

BACKUP BATT	TP73	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES
	TP74	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES

Place within 25 mm of battery connector.

RT USB	TP64	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES
	TP65	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES
	TP66	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES

Place within 25 mm of right USB connector.

LT USB	TP313	=PP5V_PWRON_LEFT_USB	10 31	FUNC_TEST=YES
	TP310	USB2_LEFT_PORT_P	11 31	FUNC_TEST=YES
	TP315	USB2_LEFT_PORT_N	11 31	FUNC_TEST=YES

Place within 25 mm of left USB connector.

Functional Test Points

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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D	051-6839	02

SCALE NONE SHT 7 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	NET_TYPE DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL 8
	I2C	I2C		I2C_PMU_SMB_SDA 8
	I2C	I2C		I2C_PMU_SCL 8
	I2C	I2C		I2C_PMU_SDA 8
I2C_NB	I2C	I2C		I2C_I2_NB_SCL 8
I2C_NB	I2C	I2C		I2C_I2_NB_SDA 8
	I2C	I2C		I2C_I2_SB_SCL 8
	I2C	I2C		I2C_I2_SB_SDA 8
	I2C	I2C		I2C_GPU_TMDS_SCL 8
	I2C	I2C		I2C_GPU_TMDS_SDA 8

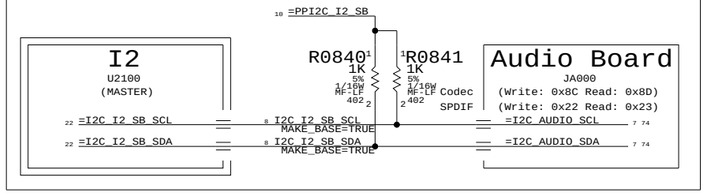
Page Notes

Power aliases required by this page:
(NONE)

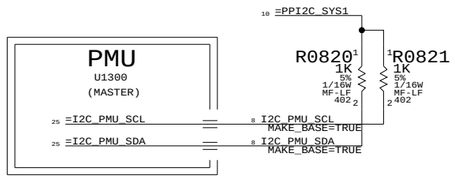
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
  Allows bypassing Governator I2C bus. Most devices are connected directly to PMU unstead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
  Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown. NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.

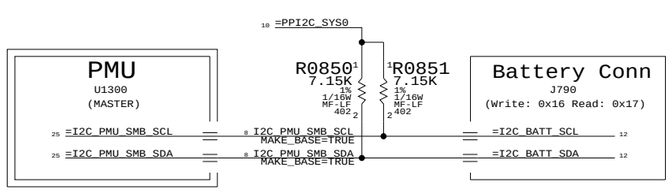
SouthBridge I2C Bus



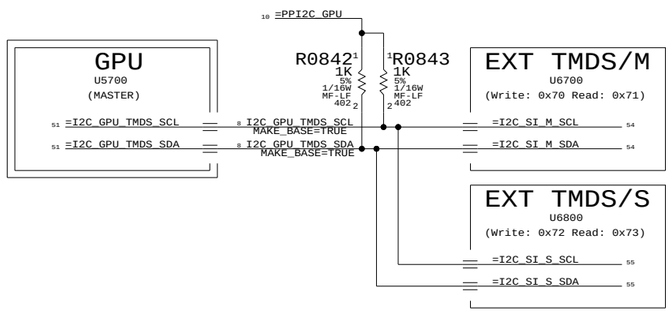
PMU I2C Bus



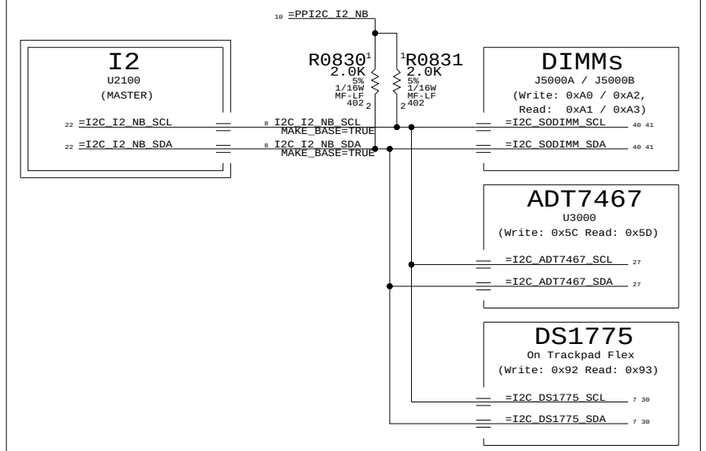
PMU SMBus



GPU I2C Bus



NorthBridge I2C Bus



I2C Connections

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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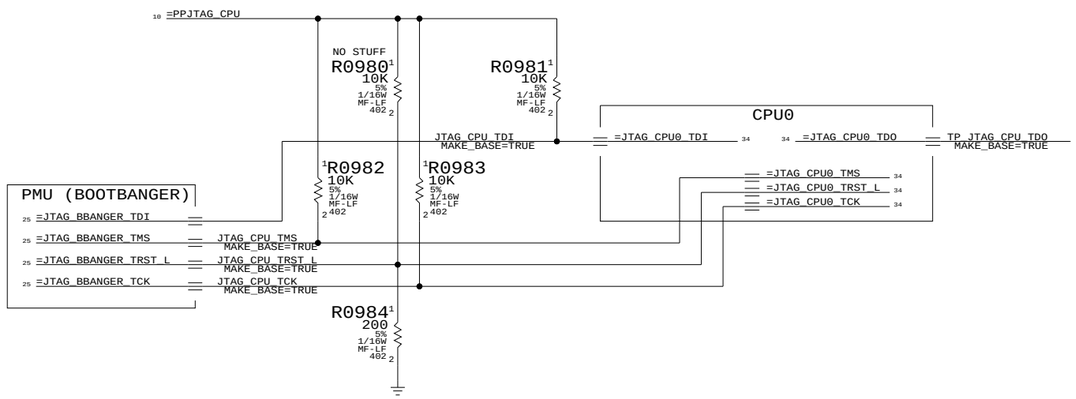
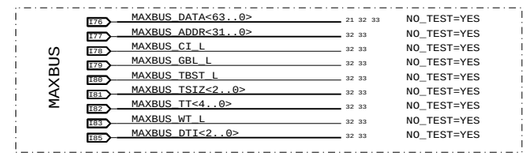
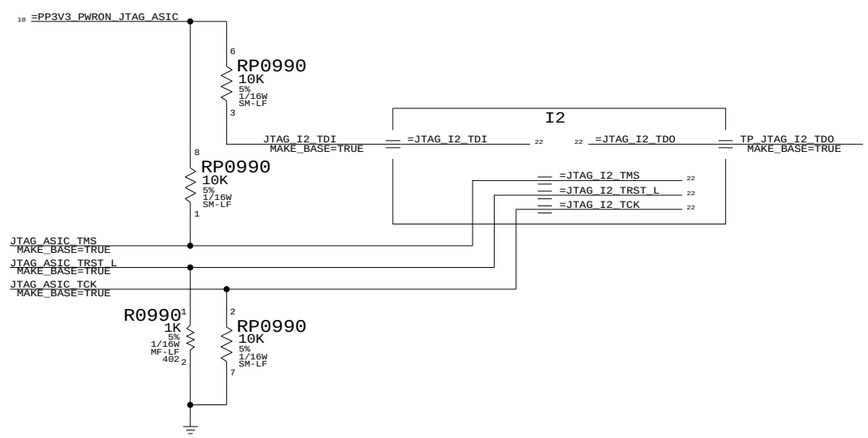
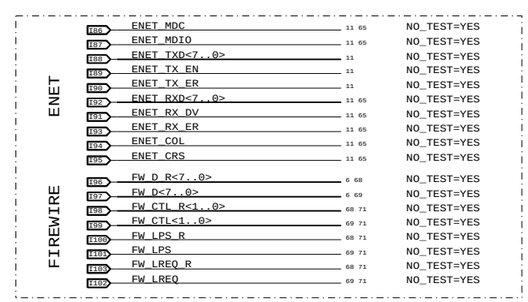
SCALE NONE	SHT 8 OF	115

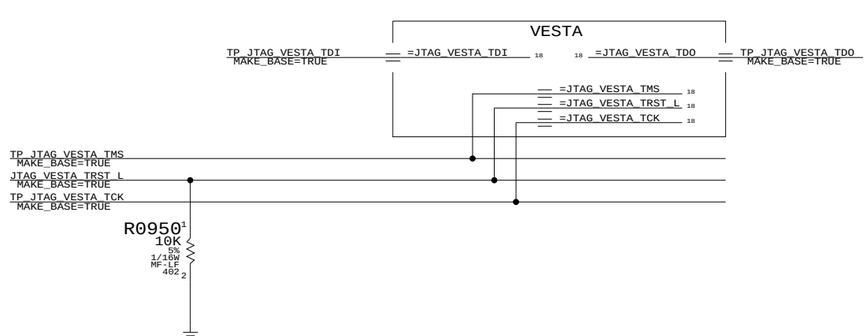


Nets not requiring TPs due to JTAG









JTAG Connections

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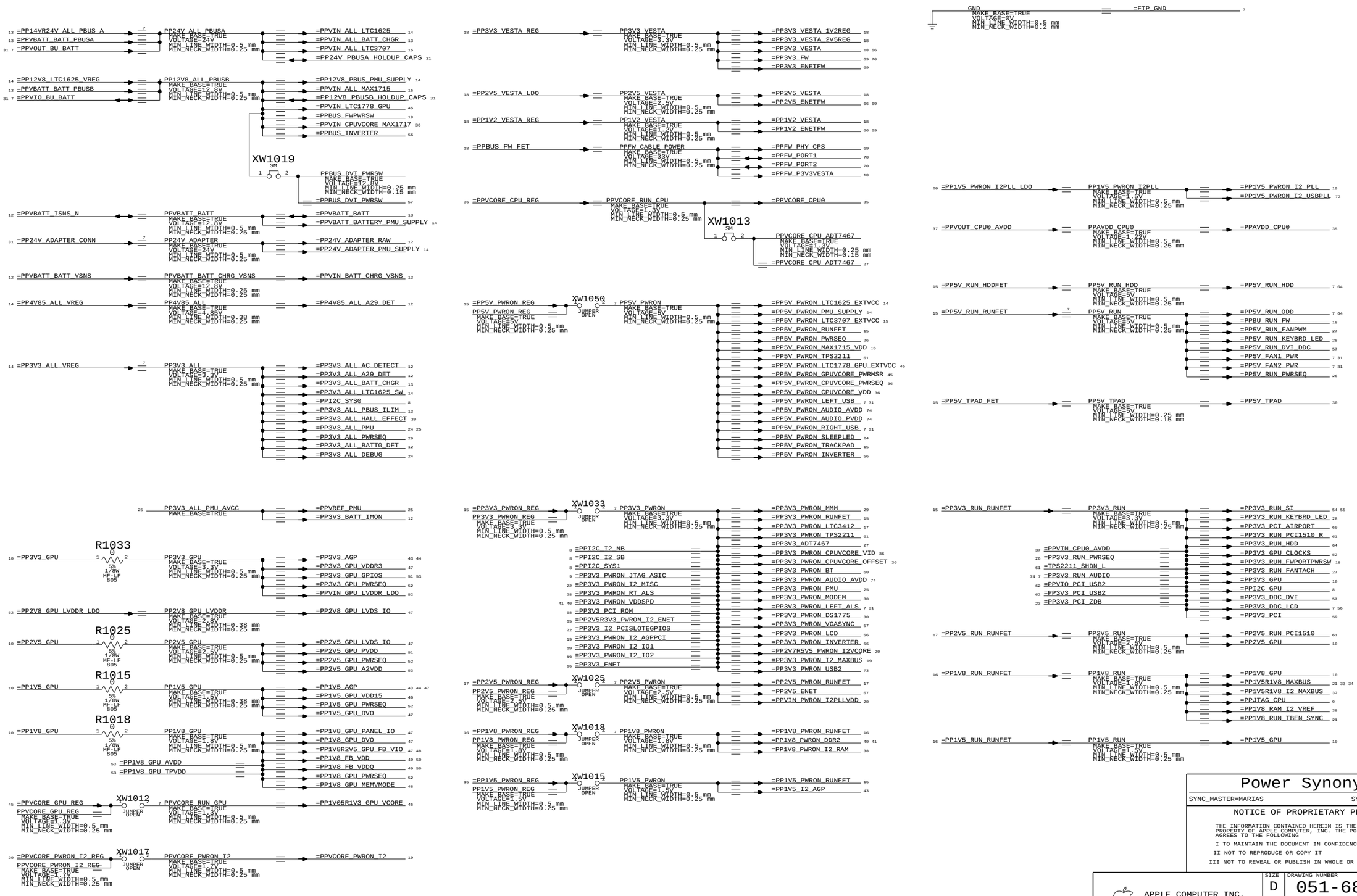
SCALE NONE SHT 9 OF 115



Power Synonyms

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D	051-6839	02

SCALE NONE SHT 10 OF 115

I2S0 Series Rs

RP1150 33 5% 1/16W SM-LF

6 =RP1150P1	1	8	=RP1150P8 6
6 =RP1150P2	2	7	=RP1150P7 6
6 =RP1150P3	3	6	=RP1150P6 6
6 =RP1150P4	4	5	=RP1150P5 6

One resistor for each of:
- I2S0_SB_TO_DEV_DTO(_R)
- I2S0_MCLK(_R)
- I2S0_BITCLK(_R)
- I2S0_SYNC(_R)

I2S1 Series Rs

RP1151 33 5% 1/16W SM-LF

6 =RP1151P1	1	8	=RP1151P8 6
6 =RP1151P2	2	7	=RP1151P7 6
6 =RP1151P3	3	6	=RP1151P6 6
6 =RP1151P4	4	5	=RP1151P5 6

One resistor for each of:
- I2S1_SB_TO_DEV_DTO(_R)
- I2S1_MCLK(_R)
- I2S1_BITCLK(_R)
- I2S1_SYNC(_R)

GPU

R1140 22 5% 1/16W MF-LF 402

43 AGP_CLK66M_GPU_R → 1 — 2 → AGP_CLK66M_GPU 44

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =AGP_GPU_RESET_L 44

AGP_VREF — MAKE_BASE=TRUE, VOLTAGE=0.75V, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.15 mm
- =I2_AGP_VREF 43
- =AGP_VREF 44
- =GPU_AGP_VREF 44

51 TP_EXTTMDS_RESET_L — SI_TMDS_RESET_L — MAKE_BASE=TRUE — =SI_TMDS_RESET_L 54 55

CPU Clocks

R1110 10 5% 1/16W MF-LF 402

32 MAXBUS_CLK_CPU0_R → 1 — 2 → MAXBUS_CLK_CPU0 — MAKE_BASE=TRUE — =MAXBUS_CPU0_CLK 33

MAXBUS_TBEN_SYNC

R1111 10 5% 1/16W MF-LF 402

32 TP_MAXBUS_CLK_CPU1_R — MAXBUS_CLK_CPU1_R — MAKE_BASE=TRUE → 1 — 2 → MAXBUS_CLK_TBEN_SYNC — MAKE_BASE=TRUE — =SYSCLK_TBEN_SYNC 21

USB Controller Mux

R1160 0 5% 1/16W MF-LF 402 — USB2_NEC
31 7 USB2_LEFT_PORT_P — USB2_NEC_LEFT_PORT_P 6 11

R1161 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_LT_PORT — USB2_I2_LEFT_PORT_P 6 11

R1162 0 5% 1/16W MF-LF 402 — USB2_NEC
31 7 USB2_LEFT_PORT_N — USB2_NEC_LEFT_PORT_N 6 11

R1163 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_LT_PORT — USB2_I2_LEFT_PORT_N 6 11

R1164 0 5% 1/16W MF-LF 402 — USB2_NEC
31 7 USB2_RIGHT_PORT_P — USB2_NEC_RIGHT_PORT_P 6 11

R1165 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_RT_PORT — USB2_I2_RIGHT_PORT_P 6 11

R1166 0 5% 1/16W MF-LF 402 — USB2_NEC
31 7 USB2_RIGHT_PORT_N — USB2_NEC_RIGHT_PORT_N 6 11

R1167 0 5% 1/16W MF-LF 402 — USB2_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB2_RT_PORT — USB2_I2_RIGHT_PORT_N 6 11

R1170 0 5% 1/16W MF-LF 402 — USB1P1_NEC
60 USB_BT_P — USB_NEC_BT_P 6 11

R1171 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_BT — USB_I2_BT_P 6 11

R1172 0 5% 1/16W MF-LF 402 — USB1P1_NEC
60 USB_BT_N — USB_NEC_BT_N 6 11

R1173 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_BT — USB_I2_BT_N 6 11

R1174 0 5% 1/16W MF-LF 402 — USB1P1_NEC
30 7 USB_TPAD_P — USB_NEC_TPAD_P 6 11

R1175 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_TPAD — USB_I2_TPAD_P 6 11

R1176 0 5% 1/16W MF-LF 402 — USB1P1_NEC
30 7 USB_TPAD_N — USB_NEC_TPAD_N 6 11

R1177 0 5% 1/16W MF-LF 402 — USB1P1_I2
NET_SPACING_TYPE=USB2, NET_PHYSICAL_TYPE=USB2, DIFFERENTIAL_PAIR=USB_TPAD — USB_I2_TPAD_N 6 11

PCI

R1120 22 5% 1/16W MF-LF 402

59 TP_PCI_CLK33M_SLOTA_R — PCI_CLK33M_ZDB_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_ZDB — MAKE_BASE=TRUE — =PCI_CLK33M_ZDB_IN 23

MAXBUS_TBEN_SYNC

R1130 22 5% 1/16W MF-LF 402

59 TP_PCI_CLK33M_SLOTD_R — PCI_CLK33M_TBEN_SYNC_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_TBEN_SYNC — MAKE_BASE=TRUE — =CLK33M_TBEN_SYNC 21

R1135 0 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<0> — PCI_CLK33M_AIRPORT_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — =PCI_CLK33M_AIRPORT 60

59 PCI_SLOTA_REQ_L ← 6 — PCI_AIRPORT_REQ_L — MAKE_BASE=TRUE — =PCI_AIRPORT_REQ_L 60
59 PCI_SLOTA_GNT_L → 6 — PCI_AIRPORT_GNT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_GNT_L 60
59 22 PCI_SLOTA_INT_L ← — PCI_AIRPORT_INT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_INT_L 60
62 61 60 59 58 PCI_AD<17> — MAKE_BASE=TRUE — =PCI_AIRPORT_IDSEL 60
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_AIRPORT_RESET_L 60

R1136 0 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<1> — PCI_CLK33M_CBUS_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_CBUS — MAKE_BASE=TRUE — =PCI_CLK33M_CBUS 61

59 PCI_SLOTD_REQ_L ← 6 — PCI_CBUS_REQ_L — MAKE_BASE=TRUE — =PCI_CBUS_REQ_L 61
59 PCI_SLOTD_GNT_L → 6 — PCI_CBUS_GNT_L — MAKE_BASE=TRUE — =PCI_CBUS_GNT_L 61
59 22 PCI_SLOTD_INT_L ← — PCI_CBUS_INT_L — MAKE_BASE=TRUE — =PCI_CBUS_INT_L 61
62 61 60 59 58 PCI_AD<20> — MAKE_BASE=TRUE — =PCI_CBUS_IDSEL 61
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_CBUS_RESET_L 61

R1137 0 5% 1/16W MF-LF 402

23 =PCI_CLK33M_ZDBOUT_R<2> — PCI_CLK33M_USB2_R — MAKE_BASE=TRUE → 1 — 2 → PCI_CLK33M_USB2 — MAKE_BASE=TRUE — =PCI_CLK33M_USB2 62

22 PCI_SLOTE_REQ_L ← — PCI_USB2_REQ_L — MAKE_BASE=TRUE — =PCI_USB2_REQ_L 62
22 PCI_SLOTE_GNT_L → — PCI_USB2_GNT_L — MAKE_BASE=TRUE — =PCI_USB2_GNT_L 62
22 PCI_SLOTE_INT_L ← — PCI_USB2_INT_L — MAKE_BASE=TRUE — =PCI_USB2_INT_L 62
62 61 60 59 PCI_AD<21> — MAKE_BASE=TRUE — =PCI_USB2_IDSEL 62
25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_USB2_RESET_L 62

23 =PCI_CLK33M_ZDBOUT_R<3> — TP_PCI_CLK33M_ZDBOUT3 — MAKE_BASE=TRUE

USB Port Assignments

11 6 USB2_I2_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<0> 72
11 6 USB2_I2_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<0> 72
11 6 USB2_I2_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<2> 72
11 6 USB2_I2_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<2> 72
11 6 USB_I2_BT_P — MAKE_BASE=TRUE — USB2_I2_P<4> 72
11 6 USB_I2_BT_N — MAKE_BASE=TRUE — USB2_I2_N<4> 72
11 6 USB_I2_TPAD_P — MAKE_BASE=TRUE — USB2_I2_P<5> 72
11 6 USB_I2_TPAD_N — MAKE_BASE=TRUE — USB2_I2_N<5> 72

11 6 USB2_NEC_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<0> 73
11 6 USB2_NEC_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<0> 73
11 6 USB2_NEC_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<1> 73
11 6 USB2_NEC_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<1> 73
11 6 USB_NEC_BT_P — MAKE_BASE=TRUE — USB2_NEC_P<2> 73
11 6 USB_NEC_BT_N — MAKE_BASE=TRUE — USB2_NEC_N<2> 73
11 6 USB_NEC_TPAD_P — MAKE_BASE=TRUE — USB2_NEC_P<3> 73
11 6 USB_NEC_TPAD_N — MAKE_BASE=TRUE — USB2_NEC_N<3> 73

PMU Connections

30 25 7 SYS_OVERTEMP_L — MAKE_BASE=TRUE — =ADT7467_THERM_L 27
13 PMU_CHARGE_V — MAKE_BASE=TRUE — TP_PMU_P7_5 25
25 PMU_CPU_HRESET_L — MAKE_BASE=TRUE — =CPU_HRESET_L 34
12 SYS_PMU_ANALOG_AC_DET — MAKE_BASE=TRUE — TP_PMU_AN_P10_6 25
25 GOV_RESET_L — TP_GOV_RESET_L — MAKE_BASE=TRUE
25 PMU_CPU_CLK_EN — MAKE_BASE=TRUE — =I2_STOPCPU_L 22
25 PMU_SYS_CLK_EN — MAKE_BASE=TRUE — =I2_STOPXTAL_L 22

26 SYS_PWRSEQ_1 — MAKE_BASE=TRUE — TP_PMU_AN_P0_1 25
26 SYS_PWRSEQ_2 — MAKE_BASE=TRUE — TP_PMU_AN_P0_2 25
26 SYS_PWRSEQ_3_L — MAKE_BASE=TRUE — TP_PMU_AN_P0_3 25
26 SYS_PWRSEQ_4 — MAKE_BASE=TRUE — TP_PMU_AN_P0_4 25
26 SYS_PWRSEQ_5 — MAKE_BASE=TRUE — TP_PMU_AN_P0_5 25
26 SYS_PWRSEQ_6_L — MAKE_BASE=TRUE — TP_PMU_P7_4 25
26 SYS_PWRSEQ_FINAL — MAKE_BASE=TRUE — TP_PMU_AN_P10_5 25

110 TP_PMU_P3_0 — MAKE_BASE=TRUE 25
110 TP_PMU_P3_1 — MAKE_BASE=TRUE 25
110 TP_PMU_P3_2 — MAKE_BASE=TRUE 25
110 TP_PMU_P3_3 — MAKE_BASE=TRUE 25

Vesta Ethernet

65 ENET_TX_EN_R → 9 — ENET_TX_EN — MAKE_BASE=TRUE → =ENET_TX_EN 66
65 ENET_TX_ER_R → 9 — ENET_TX_ER — MAKE_BASE=TRUE → =ENET_TX_ER 66
65 ENET_TXD_R<7..0> → 9 — ENET_TXD<7..0> — MAKE_BASE=TRUE → =ENET_TXD<7..0> 66
65 ENET_RESET_L → R1185 100K 5% 1/16W MF-LF 402 (1, 2)

65 9 ENET_RXD<7..0> — MAKE_BASE=TRUE ← =ENET_RXD_R<7..0> 66
65 9 ENET_RX_DV — MAKE_BASE=TRUE ← =ENET_RX_DV_R 66
65 9 ENET_RX_ER — MAKE_BASE=TRUE ← =ENET_RX_ER_R 66
65 9 ENET_COL — MAKE_BASE=TRUE ← =ENET_COL_R 66
65 9 ENET_CRS — MAKE_BASE=TRUE ← =ENET_CRS_R 66
65 ENET_CLK125M_GBE_REF — MAKE_BASE=TRUE ← =VESTA_CLK125M_GBE_REF 66
65 ENET_CLK125M_RX — MAKE_BASE=TRUE ← =VESTA_CLK125M_RX 66
65 ENET_CLK25M_TX — MAKE_BASE=TRUE ← =VESTA_CLK25M_TX 66
65 9 ENET_MDC — MAKE_BASE=TRUE ← =VESTA_MDC 66
65 9 ENET_MDIO — MAKE_BASE=TRUE ↔ =VESTA_MDIO 66
TP_ENET_ENERGYDET — MAKE_BASE=TRUE ← =VESTA_ENERGYDET 66

MISC

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =ROM_PWD_L 58
32 TP_MAXBUS_CPU1_QACK_L — NC_MAXBUS_CPU1_QACK_L — MAKE_BASE=TRUE, NO_TEST=YES
22 I2_GPIO_11 — TP_I2_GPIO_11 — MAKE_BASE=TRUE
22 I2_GPIO_EXT_02 → CPU0_VID_AB_SEL — MAKE_BASE=TRUE → =CPU0_VID_AB_SEL 36
22 =SPI_I2_REQ → CPU0_MAX1717_AB_SEL — MAKE_BASE=TRUE → =CPU0_MAX1717_AB_SEL 36
24 =SLEEP_LED_IOUT → SLEEP_LED_IOUT — MAKE_BASE=TRUE, MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm → =SLEEP_LED_CONN 74

Signal Synonyms

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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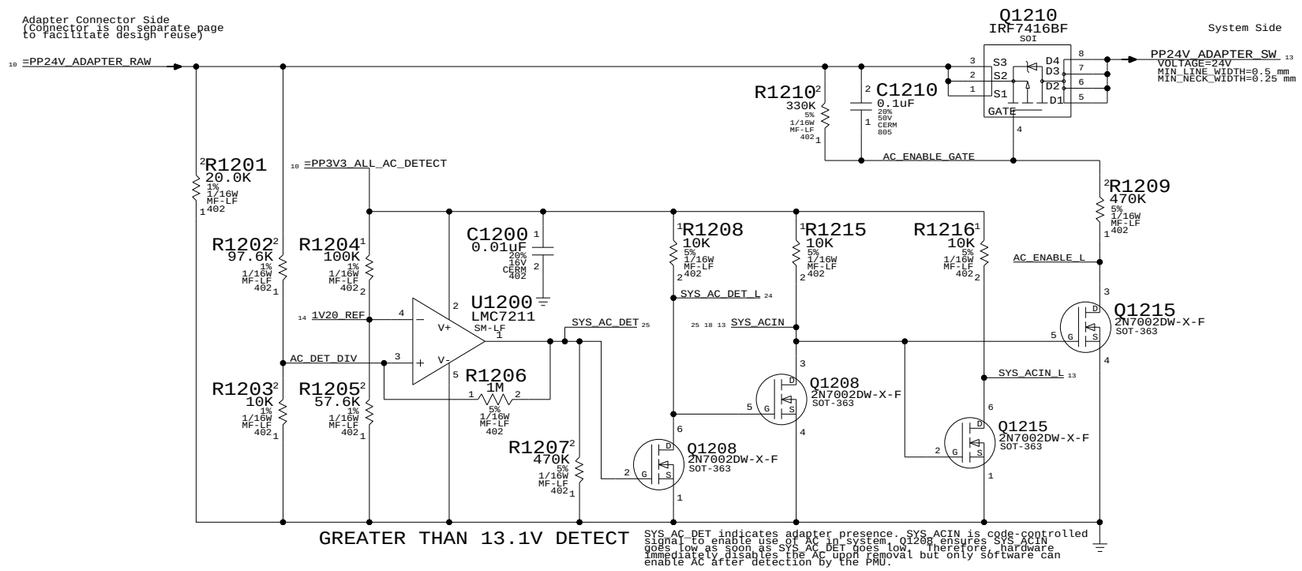
SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 11 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PBA17	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP 12
PBA18	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN 12

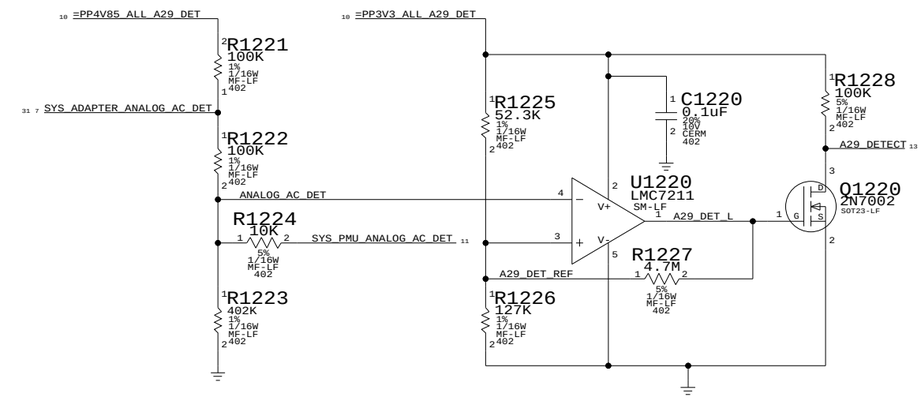
ADAPTER INPUT/INRUSH LIMITER



GREATER THAN 13.1V DETECT

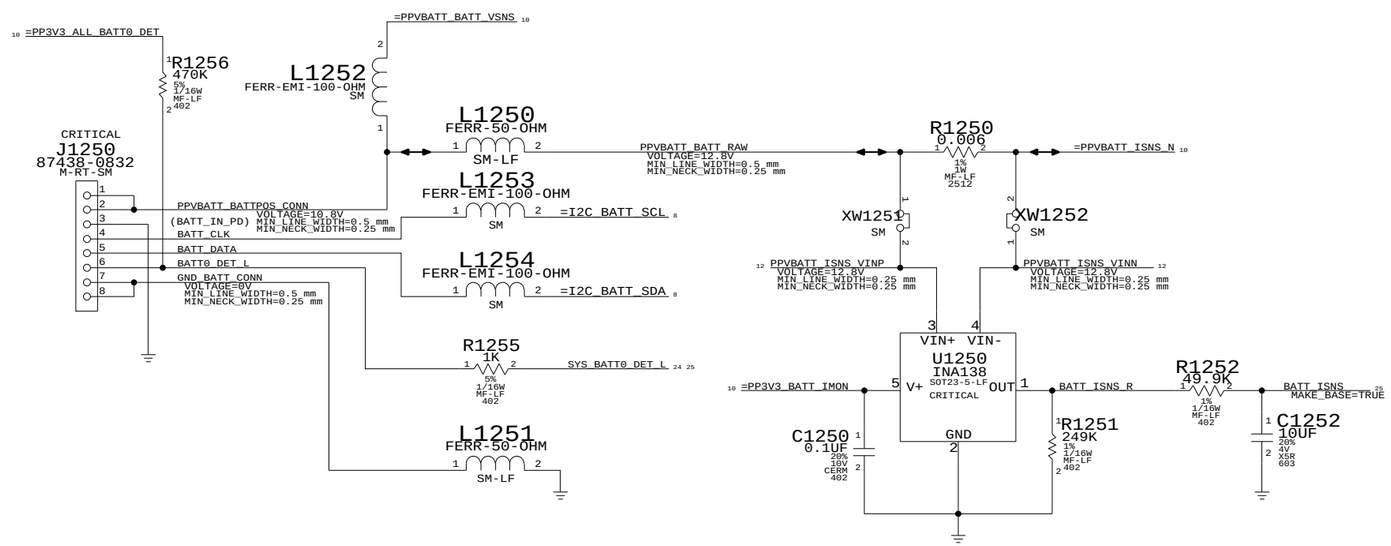
SYS_AC_DET indicates adapter presence. SYS_ACIN is code-controlled signal to enable use of AC in system. Q1208 ensures SYS_ACIN goes low as soon as SYS_AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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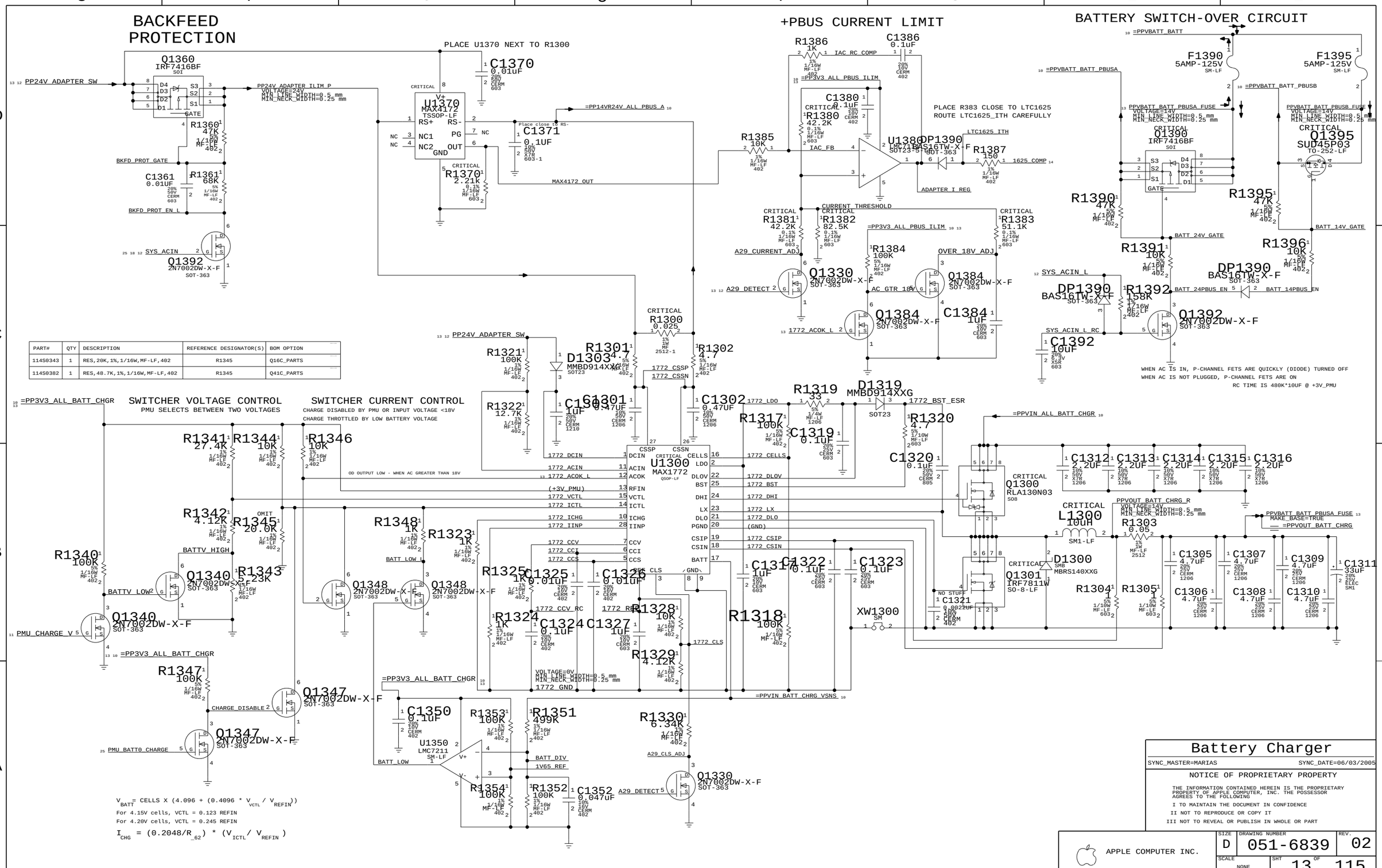
SCALE NONE	SHT 12 OF 115	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
114S0382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

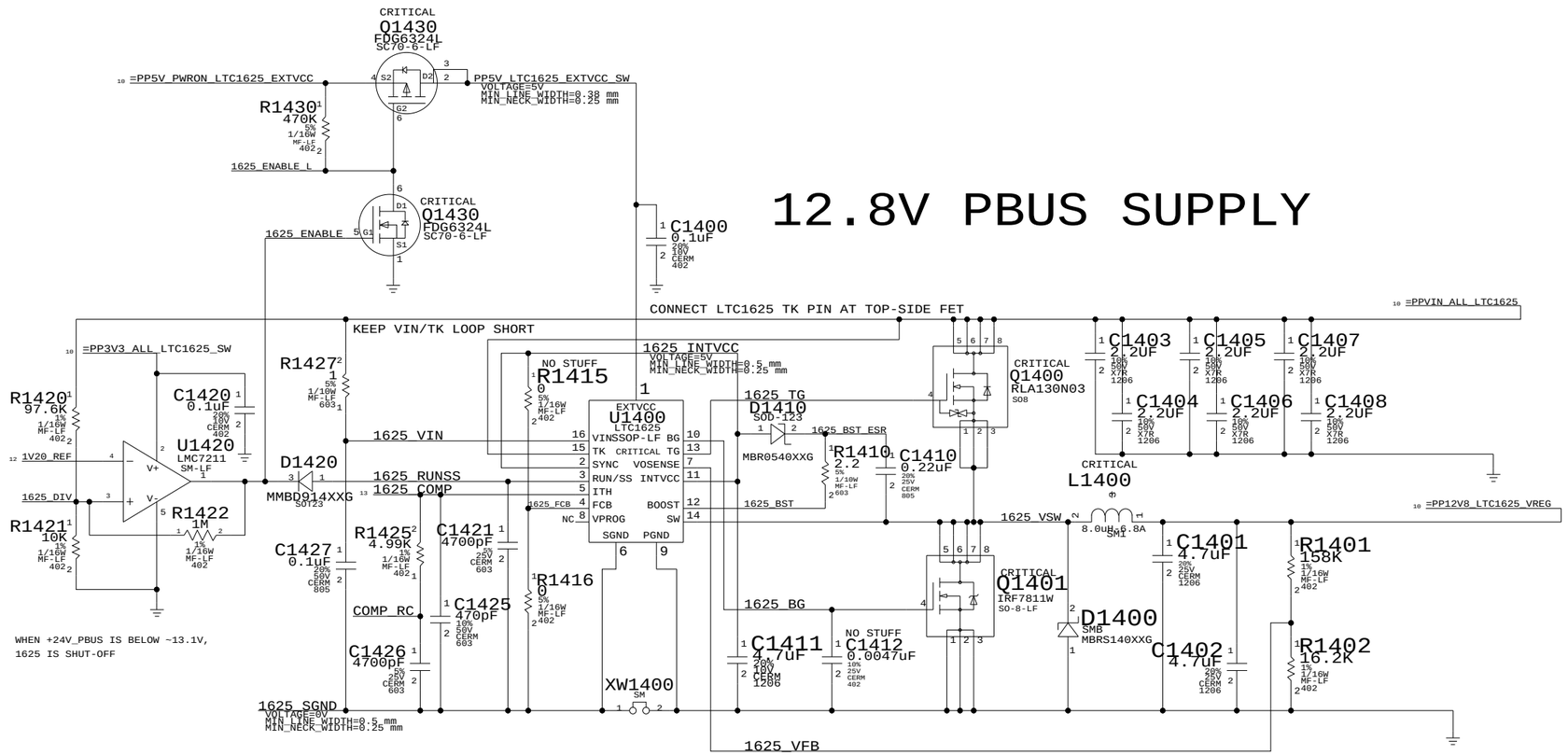
$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

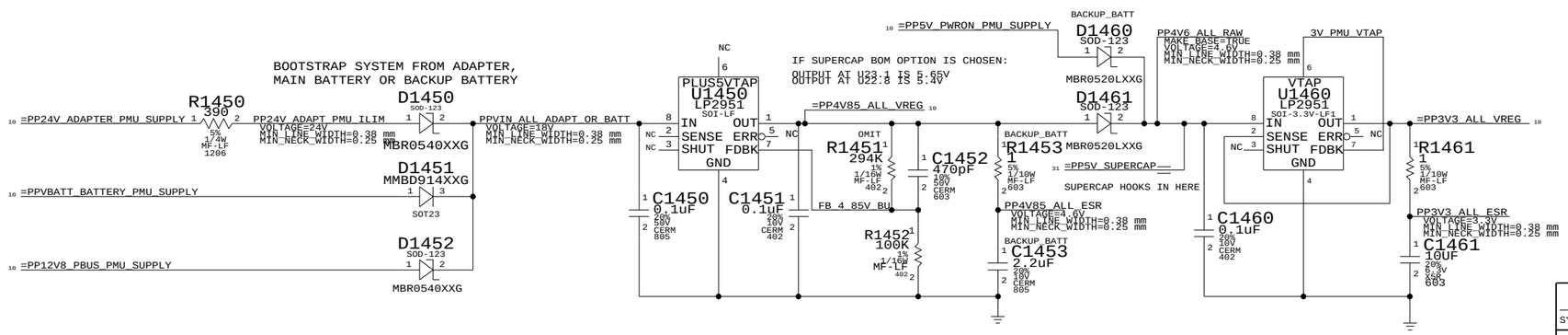
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

12.8V PBUS SUPPLY



PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2945	1	RES,MF,1/16W,394K OHM,1%,0402,SMD	R1451	?	BACKUP_BATT
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

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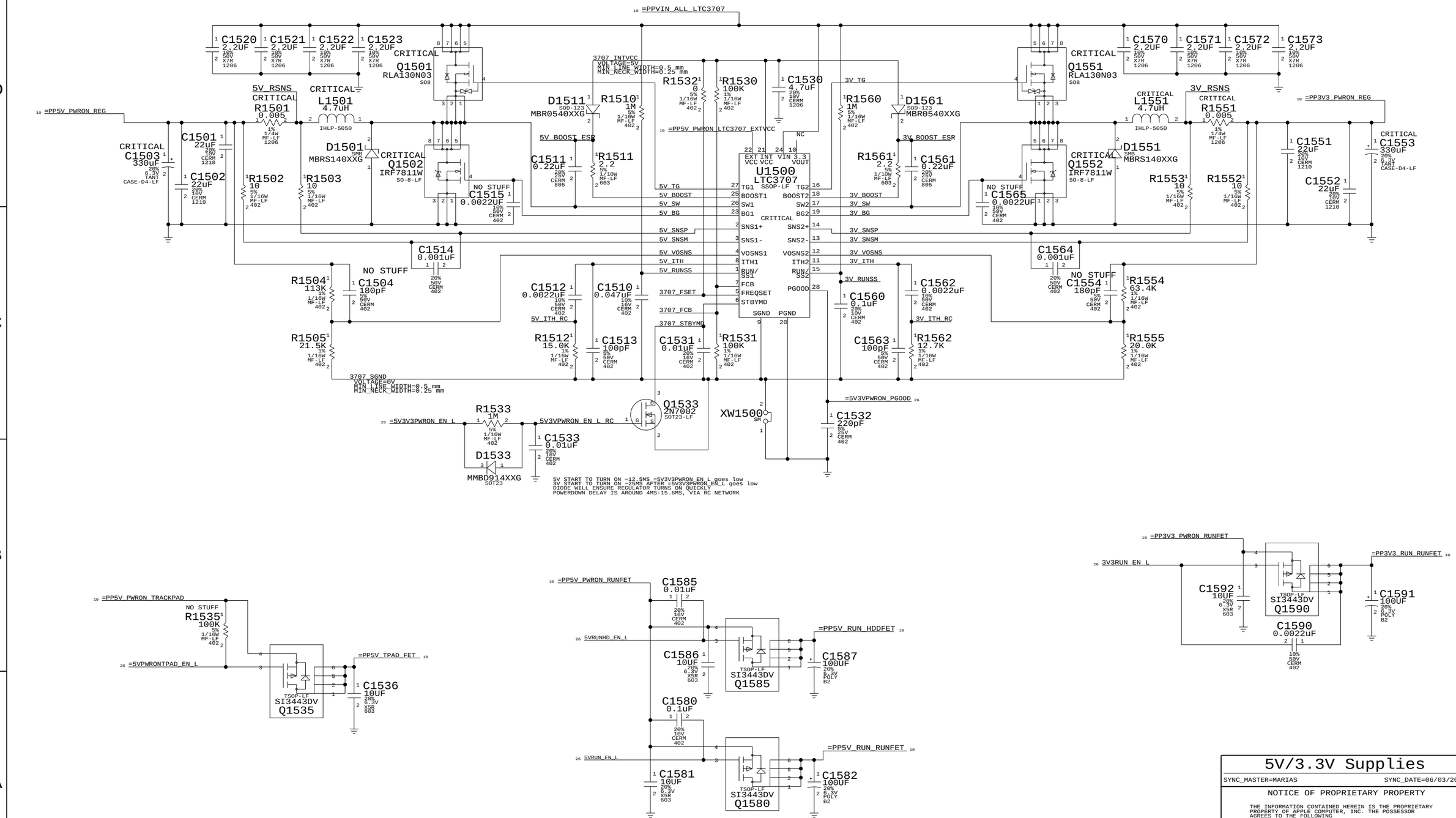
SIZE	DRAWING NUMBER	REV.
D	051-6839	02

SCALE NONE SHT 14 OF 115

3.3V/5V SWITCHER



5V/3.3V Supplies

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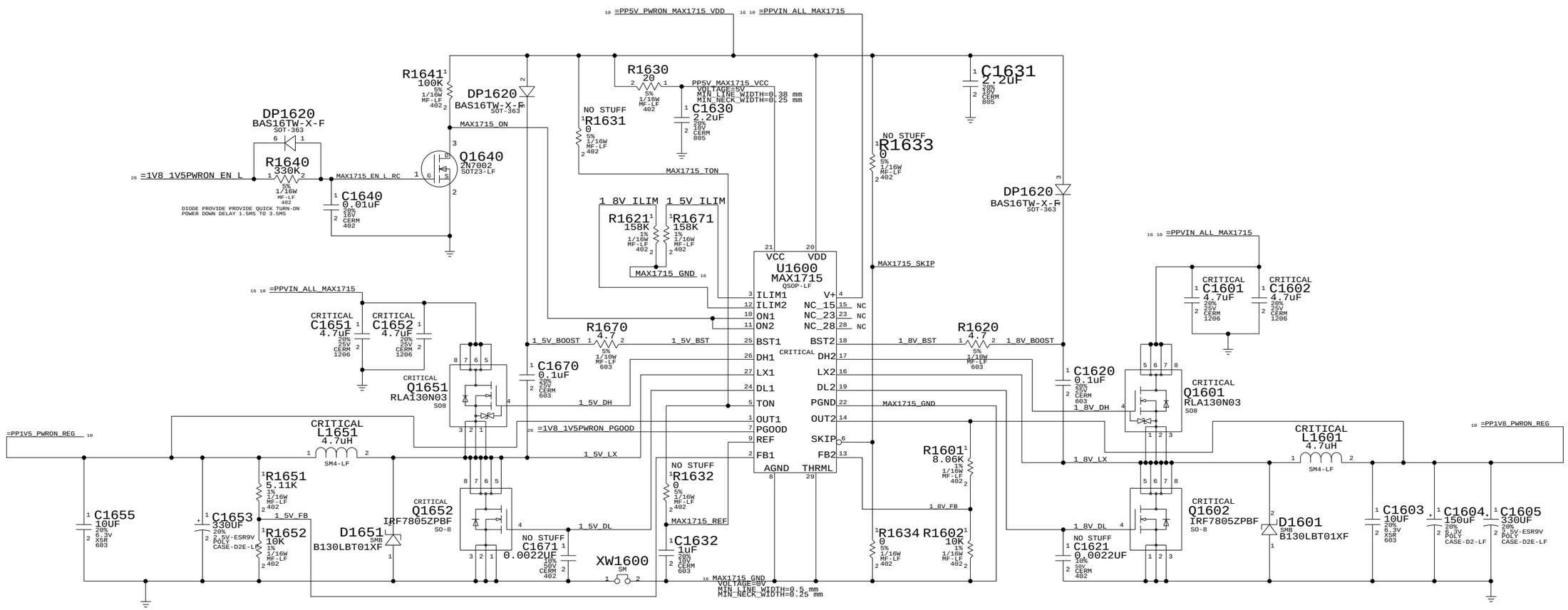
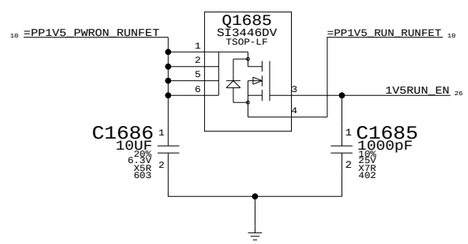
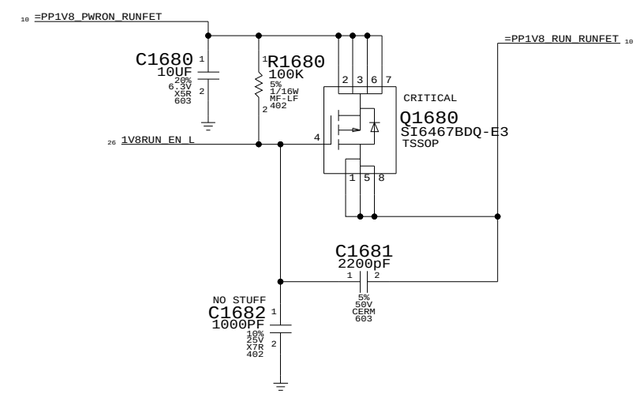
D	051-6839	02
SCALE NONE	SHT 15 OF 115	

1.5V/1.8V SWITCHER







1.8V/1.5V Supplies

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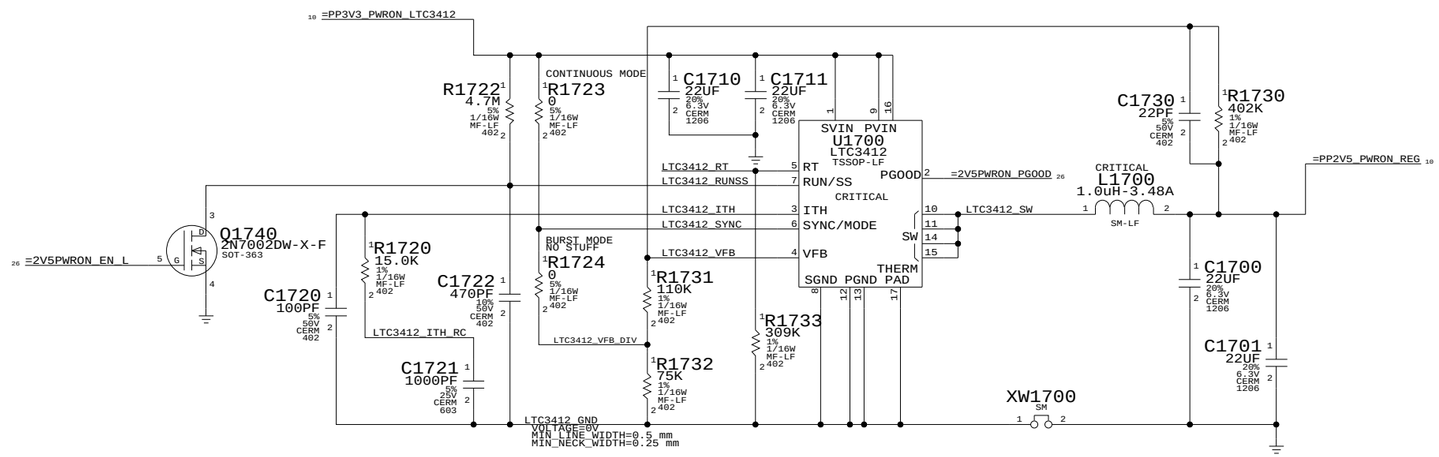
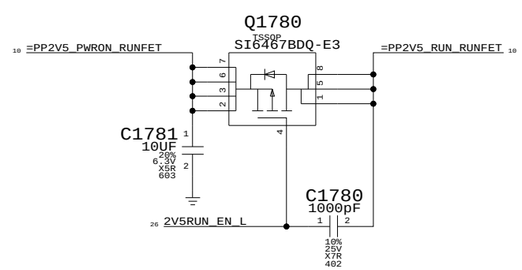
SIZE	DRAWING NUMBER	REV.
D	051-6839	02

SCALE NONE SHT 16 OF 115

2.5V SWITCHER





2.5V Supply

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 17 OF 115	

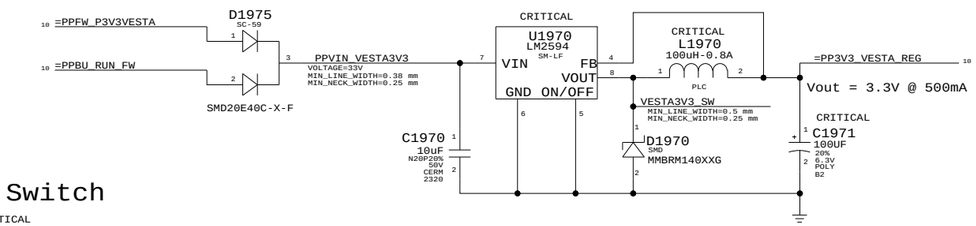
Page Notes

Power aliases required by this page:
- =PPBUS_FW (system supply for bus power)
- =PPBU_RUN_FW (backup PHY power)
- =PP3V3_RUN_FWPORTPWRSW

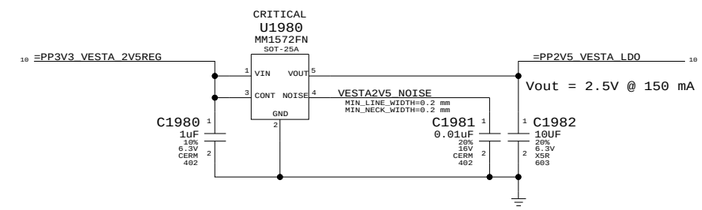
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

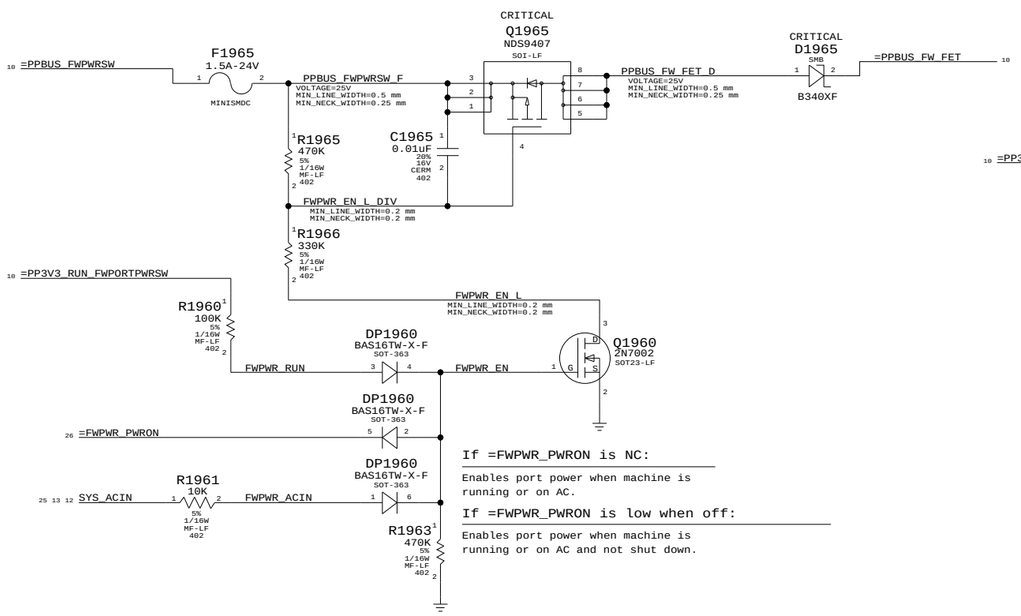
3.3V Regulator



2.5V LDO



Port Power Switch



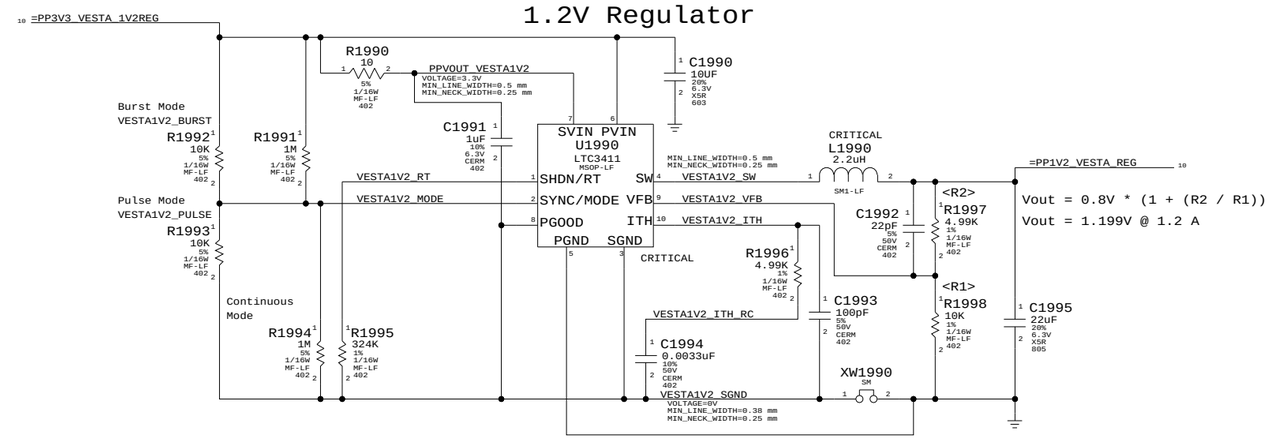
If =FWPWR_PWRON is NC:

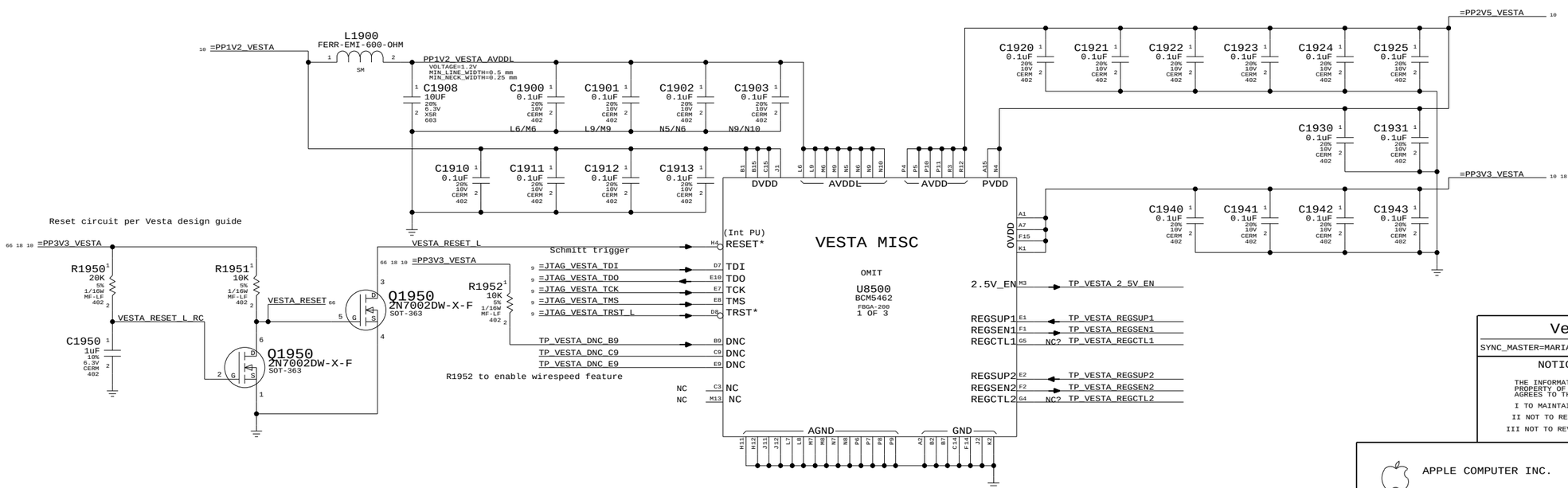
Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

1.2V Regulator





Vesta Power & Misc	
SYNC_MASTER=MARIAS	SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
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Page Notes

Power aliases required by this page:
- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.
NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

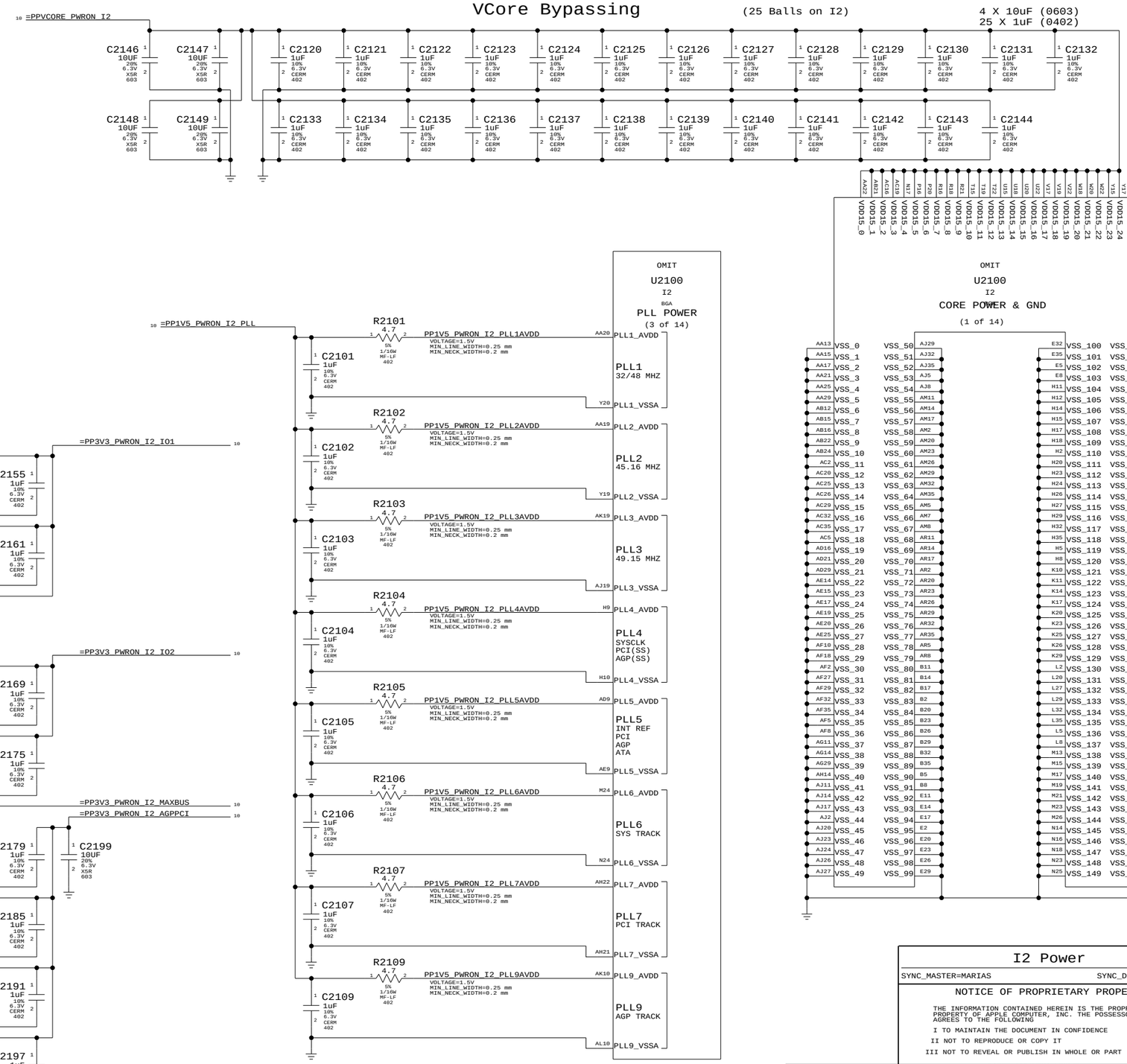
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCore Bypassing

(25 Balls on I2)

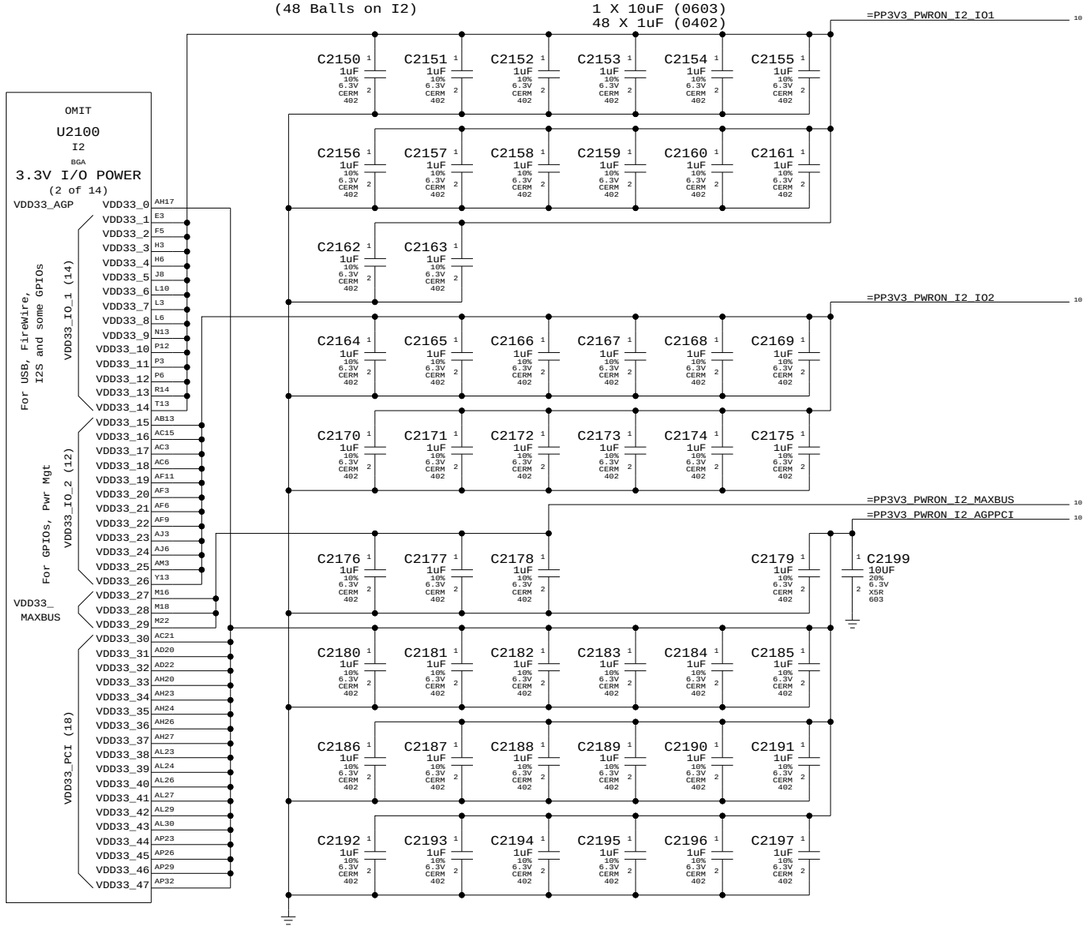
4 X 10uF (0603)
25 X 1uF (0402)



3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)



I2 Power

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
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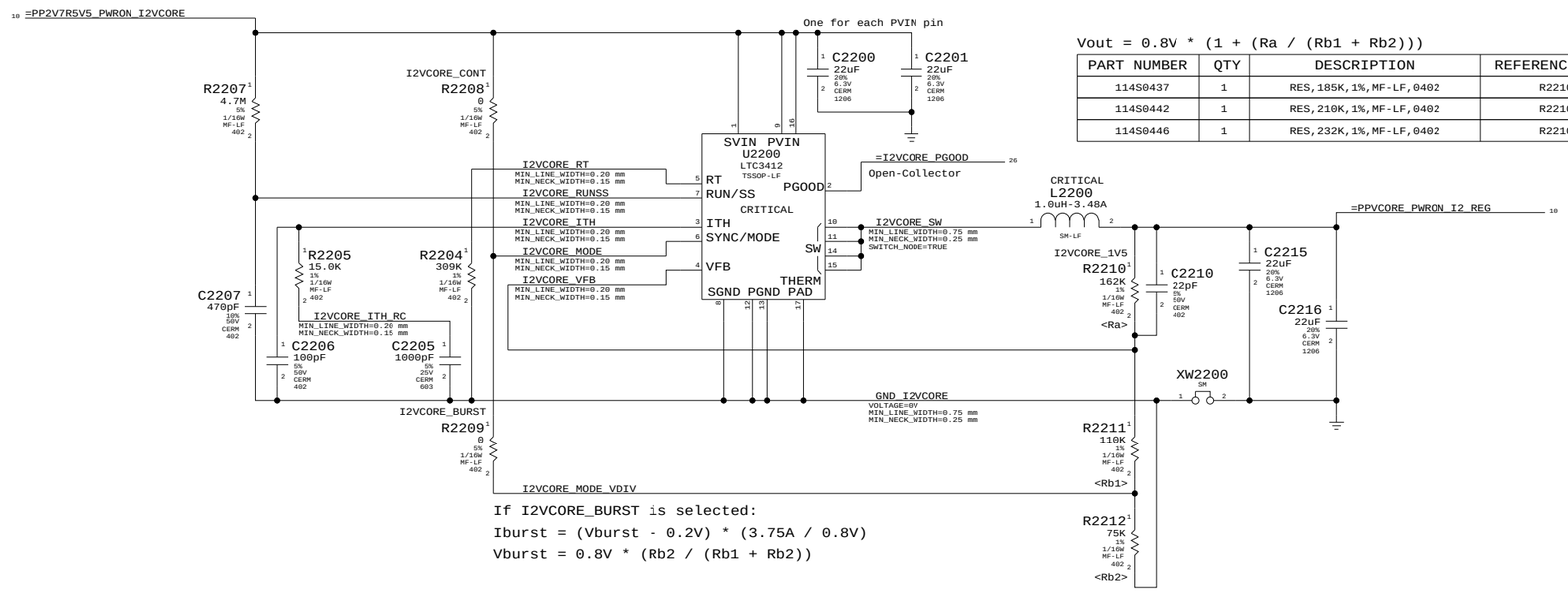
Page Notes

Power aliases required by this page:
- =PP2V7R5V5_PWRON_I2VCORE
- =PPVCORE_PWRON_I2_REG
- =PPVIN_PWRON_I2PLLVDD
- =PP1V5_PWRON_I2PLLVDD_LDO

Signal aliases required by this page:
- =I2VCORE_PGOOD

BOM options provided by this page:
- I2VCORE_CONT / I2VCORE_BURST
  Selects between forced continuous and burst mode for LTC3412 regulator.
- I2VCORE_xVx
  Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator



Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

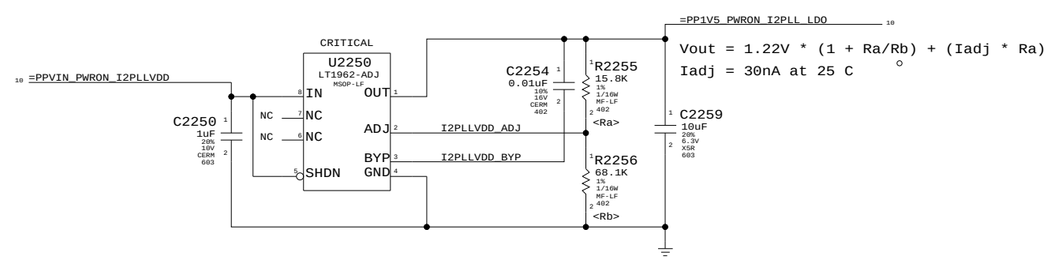
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0437	1	RES,185K,1%,MF-LF,0402	R2210		I2VCORE_1V6
114S0442	1	RES,210K,1%,MF-LF,0402	R2210		I2VCORE_1V7
114S0446	1	RES,232K,1%,MF-LF,0402	R2210		I2VCORE_1V8

If I2VCORE_BURST is selected:

Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)

Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))

I2 PLL LDO



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)

Iadj = 30nA at 25 C

I2 Power Supplies

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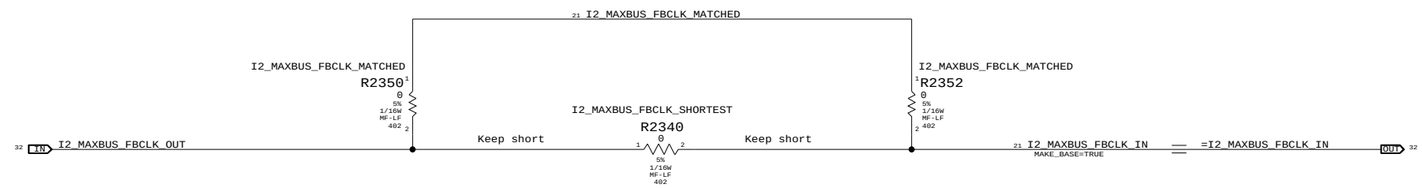
D	051-6839	02

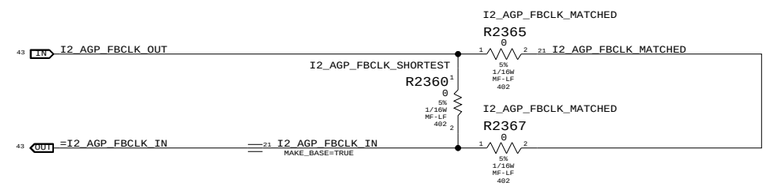
SCALE NONE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_MATCHED 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_IN 21
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_MATCHED 21
I100	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_IN 21
I100	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_MATCHED 21
I110	CLOCK	CLOCK		=CLK33M_TBEN_SYNC 11 21
I120	CLOCK	CLOCK		=SYSCLK_TBEN_SYNC 11 21

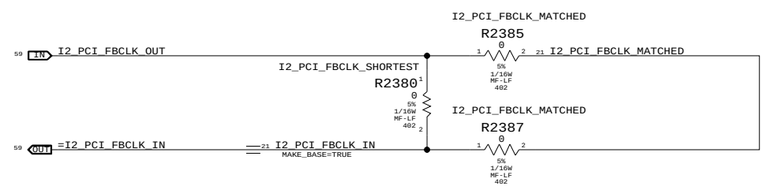
MaxBus Feedback Clock Network



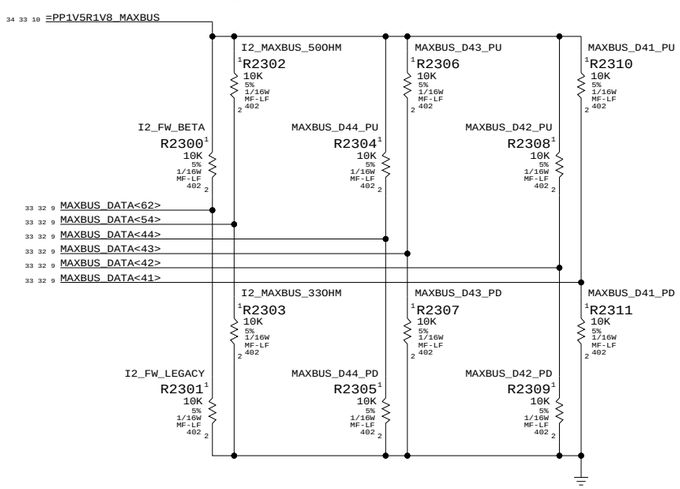
AGP Feedback Clock Ladder

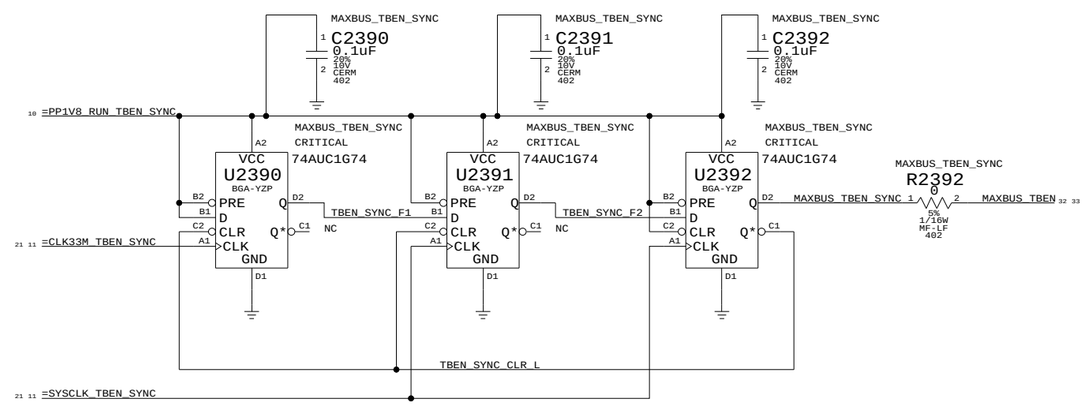


PCI Feedback Clock Ladder



I2 Configuration Straps





Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>	See Table Below	

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PU

I2 Supplemental

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTI	I2S	I2S	
I2S0_DTO	I2S	I2S	
I2S0_MCLK	I2S	I2S	
I2S0_BITCLK	I2S	I2S	
I2S0_SYNC	I2S	I2S	
I2S1_DTI	I2S	I2S	
I2S1_DTO	I2S	I2S	
I2S1_MCLK	I2S	I2S	
I2S1_BITCLK	I2S	I2S	
I2S1_SYNC	I2S	I2S	
I2_XTAL	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	

I2S0_DEV_TO_SB_DTI 7 22 74
I2S0_SB_TO_DEV_DTO_R 6 22
I2S0_MCLK_R 6 22
I2S0_BITCLK_R 6 22
I2S0_SYNC_R 6 22
I2S1_DEV_TO_SB_DTI 22 30
I2S1_SB_TO_DEV_DTO_R 6 22
I2S1_MCLK_R 6 22
I2S1_BITCLK_R 6 22
I2S1_SYNC_R 6 22
I2_CLK18M_XOUT_R 22
I2_CLK18M_XOUT 22
I2_CLK18M_XIN 22

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0

GPIO Pull-ups / Pull-downs

=PP3V3_PWRON_I2_MISC 10 22
=PP3V3_I2_PCISLOTEGPIOS 10

EXT_00	Internal pull-up to 3.3V PWRON
EXT_01	Internal pull-up to 3.3V PWRON
EXT_02	10K Pull-up to 3.3V on I2 AGP page.
EXT_03	Pull-up/down to be provided by audio page.
EXT_04	Pull-up/down to be provided by audio page.
EXT_05	10K Pull-up to Enet OVdd on I2 Enet page.
EXT_06	10K Pull-up to 3.3V on I2 PCI page.
EXT_07	10K Pull-up to 3.3V on I2 PCI page.
	I2_REV1_NOT
EXT_08	R2455 10K 5% 1/16W MF-LF 402 — (I2_EXT_08) PCI_SLOTE_INT_L 11 22 — (*) - Rev 1.0: Internal pull-up to 3.3V PWRON
EXT_09	Internal pull-up to 3.3V PWRON
EXT_10	Pull-up/down to be provided by audio page.
EXT_11	R2452 10K 5% 1/16W MF-LF 402 (I2_REV1) — MMM_FFIRQ_L 22 25
EXT_12	Internal pull-up to 3.3V PWRON — (*) - Rev 1.0: Missing internal pull-up to 3.3V PWRON
EXT_13	RP2450 10K 5% 1/16W SM-LF — (I2_EXT_13) PCI_SLOTE_GNT_L 11 22
EXT_14	RP2450 10K 5% 1/16W SM-LF — (I2_EXT_14) PCI_SLOTE_REQ_L 11 22
EXT_15	Pull-up/down to be provided by audio page.
EXT_16	Pull-up/down to be provided by audio page. (*) - See above
GPIO_EXT_00	Pull-up/down to be provided by audio page.
GPIO_EXT_01	RP2450 10K 5% 1/16W SM-LF — =SPI_I2_REQ 11 22
GPIO_EXT_02	R2451 10K 5% 1/16W MF-LF 402 (I2_REV1) — I2_GPIO_EXT_02 11 22 — (*) - Rev 1.0: Missing internal pull-up to 3.3V PWRON
GPIO_EXT_03	Internal pull-up to 3.3V PWRON
GPIO_04	RP2450 10K 5% 1/16W SM-LF — FW_POWERDOWN 22
GPIO_05	Pull-up/down to be provided by audio page.
GPIO_06	Pull-up/down to be provided by audio page.
GPIO_09	Pull-up/down to be provided by audio page.
GPIO_11	Internal pull-up to 3.3V PWRON
GPIO_12	Pull-up/down to be provided by audio page. (*) - See above
GPIO_15	Pull-up/down to be provided by audio page.
GPIO_16	Pull-up/down to be provided by design.

U2100 — I2 — BGA — MISCELLANEOUS (4 OF 14)

OMIT

Signal Direction | Pin Direction

GPIO INTERFACE

Signal	Pin	Pin Direction	Pin	Address	MPIC Int	Int PU?	Alt Func
30 25 MODEM_RING2SYS_L	AH1	EXT_00_H (Int PU)	EXT_00	0x0_0058	46 (0x2E)	Yes	PCI_REQ_2_L (When PCI1_Slot2En = 10)
25 PMU_INT_L	AK4	EXT_01_H (Int PU)	EXT_01	0x0_0059	47 (0x2F)	Yes	
44 43 AGP_INT_L	AT19	EXT_02_H	EXT_02	0x0_005A	48 (0x30)	No	
74 7 AUDIO_LI_OPTICAL_PLUG_L	AH2	EXT_03_H	EXT_03	0x0_005B	49 (0x31)	No	
74 7 AUDIO_LI_DET_L	J2	EXT_04_H	EXT_04	0x0_005C	50 (0x32)	No	
		EXT_05_H - See Ethernet Sym	EXT_05	0x0_005D	51 (0x33)	No	
59 11 PCI_SLOTA_INT_L	AR33	EXT_06_H	EXT_06	0x0_005E	52 (0x34)	No	
59 11 PCI_SLOTD_INT_L	AN33	EXT_07_H	EXT_07	0x0_005F	53 (0x35)	No	
I2_EXT_08	AG4	EXT_08_H (Int PU - rev 1)	EXT_08	0x0_0060	54 (0x36)	Yes	
25 PMU_SB_NMI_L	AK1	EXT_09_H (Int PU)	EXT_09	0x0_0061	55 (0x37)	Yes	
74 7 AUDIO_LO_OPTICAL_PLUG_L	AG1	EXT_10_H	EXT_10	0x0_0062	56 (0x38)	No	
25 22 MMM_FFIRQ_L	AG3	EXT_11_H (Int PU)	EXT_11	0x0_0063	57 (0x39)	Yes	
25 MMM_SIRQ_L	AG2	EXT_12_H (Int PU)	EXT_12	0x0_0064	58 (0x3A)	Yes	
I2_EXT_13	AF1	EXT_13_H	EXT_13	0x0_0065	59 (0x3B)	No	PCI_GNT_2_L (When PCI1_Slot2En = 11)
I2_EXT_14	AE4	EXT_14_H	EXT_14	0x0_0066	60 (0x3C)	No	PCI_REQ_2_L (When PCI1_Slot2En = 11)
74 7 AUDIO_LO_DET_L	H1	EXT_15_H	EXT_15	0x0_0067	61 (0x3D)	No	
74 7 AUDIO_GPIO_11	G4	EXT_16_H (Int PU - rev 1)	EXT_16	0x0_0068	62 (0x3F)	Yes	
74 7 AUDIO_CODEC_RESET_L	AK2	GPIO_EXT_00_H	GPIO_00	0x0_006A	14 (0x0E)	No	
22 11 =SPI_I2_REQ	AJ1	GPIO_EXT_01_H	GPIO_01	0x0_006B	15 (0x0F)	No	SPIREQ (When SPISReqEn = 1)
22 11 I2_GPIO_EXT_02	AH4	GPIO_EXT_02_H (Int PU)	GPIO_02	0x0_006C	16 (0x10)	Yes	PCI_GNT_2_L (When PCI1_Slot2En = 10)
30 MODEM_RESET_L	AH3	GPIO_EXT_03_H (Int PU)	GPIO_03	0x0_006D	17 (0x11)	Yes	
22 FW_POWERDOWN	M1	GPIO_04_H	GPIO_04	0x0_006E	N/A	No	
74 7 AUDIO_LO_MUTE_L	G3	GPIO_05_H	GPIO_05	0x0_006F	N/A	No	
74 7 AUDIO_SPKR_MUTE_L	G1	GPIO_06_H	GPIO_06	0x0_0070	N/A	No	
74 7 AUDIO_I2S_DTIB_SEL	AG8	GPIO_09_H	GPIO_09	0x0_0073	N/A	No	
11 I2_GPIO_11	G2	GPIO_11_H (Int PU)	GPIO_11	0x0_0075	N/A	Yes	
74 7 AUDIO_SPDIFRX_RESET_L	AG7	GPIO_12_H (Int PU - rev 1)	GPIO_12	0x0_0076	N/A	Yes	
74 7 AUDIO_EXT_MCLK_SEL	AG6	GPIO_15_H	GPIO_15	0x0_0079	N/A	No	
		GPIO_16_H - See Ethernet Sym	GPIO_16	0x0_007A	N/A	No	

Alternate GPIO Functions

Use MAKE_BASE to force net name

22 11 PCI_SLOTE_INT_L
22 11 PCI_SLOTE_GNT_L
22 11 PCI_SLOTE_REQ_L

I2C

IIC_CLK_0_H — J1 — =I2C_I2_NB_SCL 8
IIC_D_0_H — J3 — =I2C_I2_NB_SDA 8
IIC_CLK_2_H — F4 — =I2C_I2_SB_SCL 8
IIC_D_2_H — F1 — =I2C_I2_SB_SDA 8

I2S 0

74 22 7 I2S0_DEV_TO_SB_DTI — E1 AUD_DTI_A_H

		(Master)	(Slave)
AUD_DTO_A_H	C1		I2S0_SB_TO_DEV_DTO_R 6 22
AUD_CLKOUT_A_H	F2		I2S0_MCLK_R 6 22
AUD_BITCLK_A_H	F3		I2S0_BITCLK_R 6 22
AUD_SYNC_A_H	D2		I2S0_SYNC_R 6 22

I2S 1

30 22 I2S1_DEV_TO_SB_DTI — J5 MOD_DTI_B_H

		(Master)	(Slave)
MOD_DTO_B_H	G5		I2S1_SB_TO_DEV_DTO_R 6 22
MOD_CLKOUT_B_H	J6		I2S1_MCLK_R 6 22
MOD_BITCLK_B_H	J7		I2S1_BITCLK_R 6 22
MOD_SYNC_B_H	G6		I2S1_SYNC_R 6 22

SCCA

22 10 =PP3V3_PWRON_I2_MISC — R2490 10K 5% 1/16W MF-LF 402
24 7 SCCA_RXD — AG5 SCC_RXDA_H
SCC_TXDA_L — AE5 — SCCA_TXD_L 7 24

SCCB/VIA

25 VIA_PMU_TO_SB — AL3 SCC_RXDB_H
25 VIA_ACK_L — AM1 SCC_GPIOB_L
25 VIA_CLK — AL1 SCC_TRXCB_H
SCC_TXDB_L — AL2 — VIA_SB_TO_PMU 25
SCC_RTSB_L — AL4 — VIA_REQ_L 25

TEST/JTAG

I2_TST_TEI — AL6 TST_TEI_H
I2_TST_PLLEN — AL5 TST_PLLEN_H
=SPI_I2_MOSI
9 =JTAG_I2_TDI — AN6 JTG_TDI_H
9 =JTAG_I2_TMS — AN2 JTG_TMS_H
9 =JTAG_I2_TCK — AN3 JTG_TCK_H
9 =JTAG_I2_TRST_L — AP1 JTG_TRSTN_L
=SPI_I2_CLK
JTG_TDO_H — AN4 — =SPI_I2_MISO / =JTAG_I2_TDO 9

R2400 10K 5% 1/16W MF-LF 402 — R2401 10K 5% 1/16W MF-LF 402

POWER MGMT/CLOCK

62 25 SYS_WARM_RESET_L — AK3 REF_PURESET_L
11 =I2_STOPXTAL_L — AH7 PWR_STPXTL_L
11 =I2_STOPCPU_L — AH6 PWR_STPCPU_L
PWR_PCI_PME_L — AK7 — SYS_PME_L 25 62
PWR_INTRWD_H — AL7 — SYS_WATCHDOG 25
25 NB_SUSPENDREQ_L — AH5 PWR_SPDREQ_L
PWR_SPDACK_L — AK5 — NB_SUSPENDACK_L 25
PWR_PENDINT_H — AK6 — TP_I2_PENDINT

Put crystal circuit close to I2

22 I2_CLK18M_XOUT_R — AC12 REF_CLK_OUT
22 I2_CLK18M_XIN — AC13 REF_CLK_IN

NO STUFF
R2410 10M 5% 1/16W MF-LF 402
R2411 0 5% 1/16W MF-LF 402
CRITICAL Y2410 18.432M 8X4.5MM-SM1
22 I2_CLK18M_XOUT
C2411 22pF 5% 50V CERM 402
C2410 22pF 5% 50V CERM 402

Crystal load capacitance is 16pF

I2 Miscellaneous

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SCALE NONE	SHT 24 OF 115	

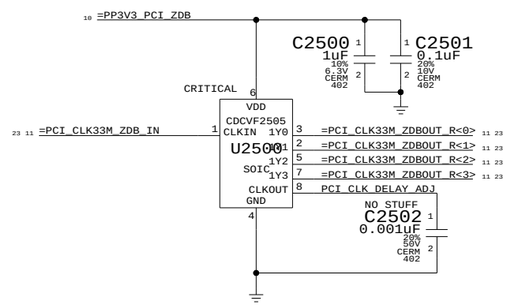
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
172	CLOCK	CLOCK		=PCI_CLK33M_ZDB_IN 11 23
173 PCI_ZDBOUT0	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<0> 11 23
174 PCI_ZDBOUT1	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<1> 11 23
175 PCI_ZDBOUT2	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<2> 11 23
176 PCI_ZDBOUT3	CLOCK	CLOCK		=PCI_CLK33M_ZDBOUT_R<3> 11 23

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0



PCI Clock Buffer

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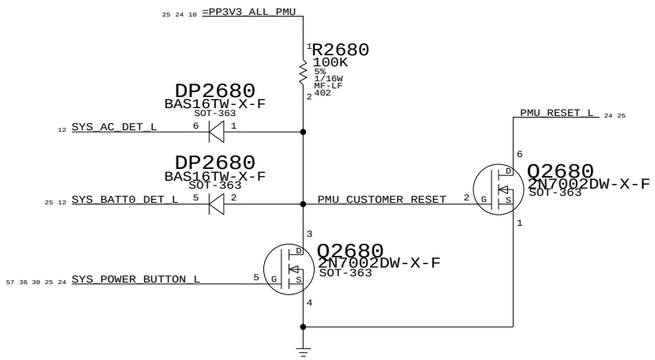
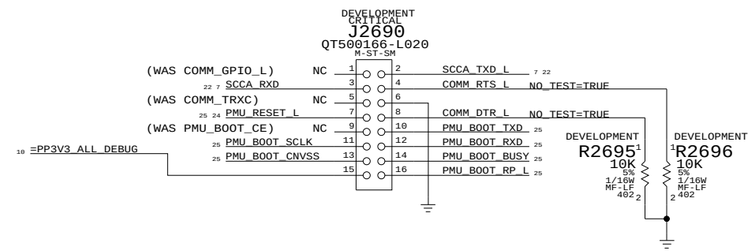
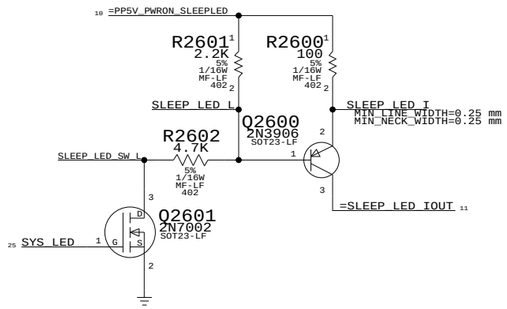
PMU RESET CIRCUIT



SERIAL DEBUG INTERFACE

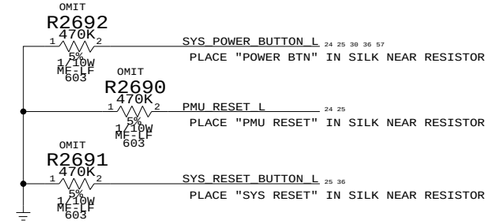


SLEEP LED

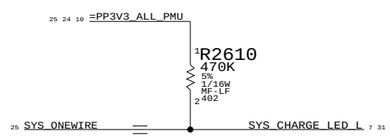


DEBUGGING AIDS

PLACE ON TOP SIDE NEAR FRONT EDGE OF BOARD



CHARGE LED



LEDs/Reset/Debug

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SCALE NONE	SHT 26 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
PMU_CLK10M_XTAL	XTAL	XTAL		PMU_CLK10M_XIN 25
	XTAL	XTAL		PMU_CLK10M_XOUT 25
	XTAL	XTAL		PMU_CLK10M_XOUT_R 25
PMU_CLK32K_XTAL	XTAL	XTAL		PMU_CLK32K_XIN 25
	XTAL	XTAL		PMU_CLK32K_XOUT 25
	XTAL	XTAL		PMU_CLK32K_XOUT_R 25

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

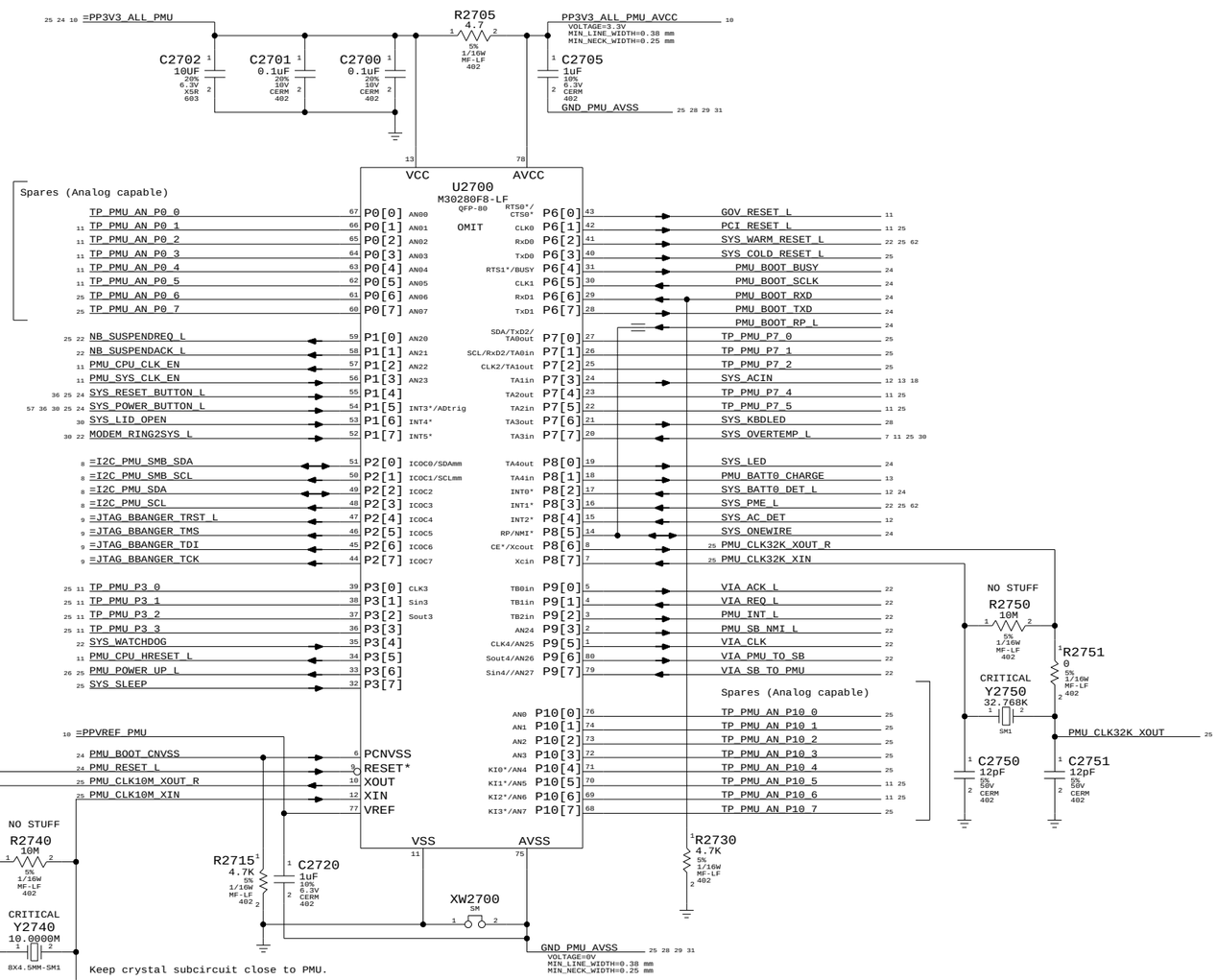
NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
(NONE)

NOTE: TP_PMU_Px_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Px_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

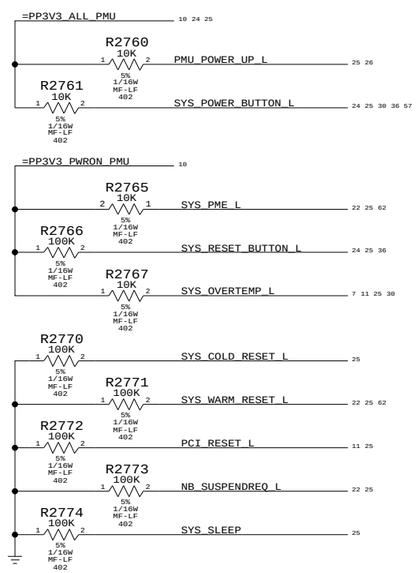
Power Management Unit



Keep crystal subcircuit close to PMU.

Y2740's load capacitance is 12pF

PMU Pull-ups / pull-downs



Additional PMU05 "Modules"

MMM

TP_PMU_AN_P10_0	MMM_X_AXIS
TP_PMU_AN_P10_1	MMM_Y_AXIS
TP_PMU_AN_P10_2	MMM_Z_AXIS
TP_PMU_P7_0	MMM_FFIRQ_L
TP_PMU_P7_1	MMM_SIRQ_L
TP_PMU_AN_P0_7	MMM_ACC_SELFTEST
TP_PMU_AN_P0_6	MMM_ACC_PWRDOWN

ALS

TP_PMU_AN_P10_3	ALS_0_OUT
TP_PMU_AN_P10_4	ALS_1_OUT
TP_PMU_P7_2	ALS_GAIN_BOOST

CPU T-Diodes

TP_PMU_AN_P10_5	CPU0_TEMP
TP_PMU_AN_P10_6	CPU1_TEMP

SPI Dual Battery Charger

TP_PMU_P3_0	SPI_PMU_CHGR_CLK
TP_PMU_P3_1	SPI_CHGR_TO_PMU_MISO
TP_PMU_P3_2	SPI_PMU_TO_CHGR_MOSI
TP_PMU_P3_3	SPI_PMU_CHGR_CS
TP_PMU_P7_4	PMU_BATT1_DET_L
TP_PMU_P7_5	PMU_BATT1_CHARGE

Battery Current Mon

TP_PMU_AN_P10_7	BATT_ISNS

Power Management Unit (PMU05)

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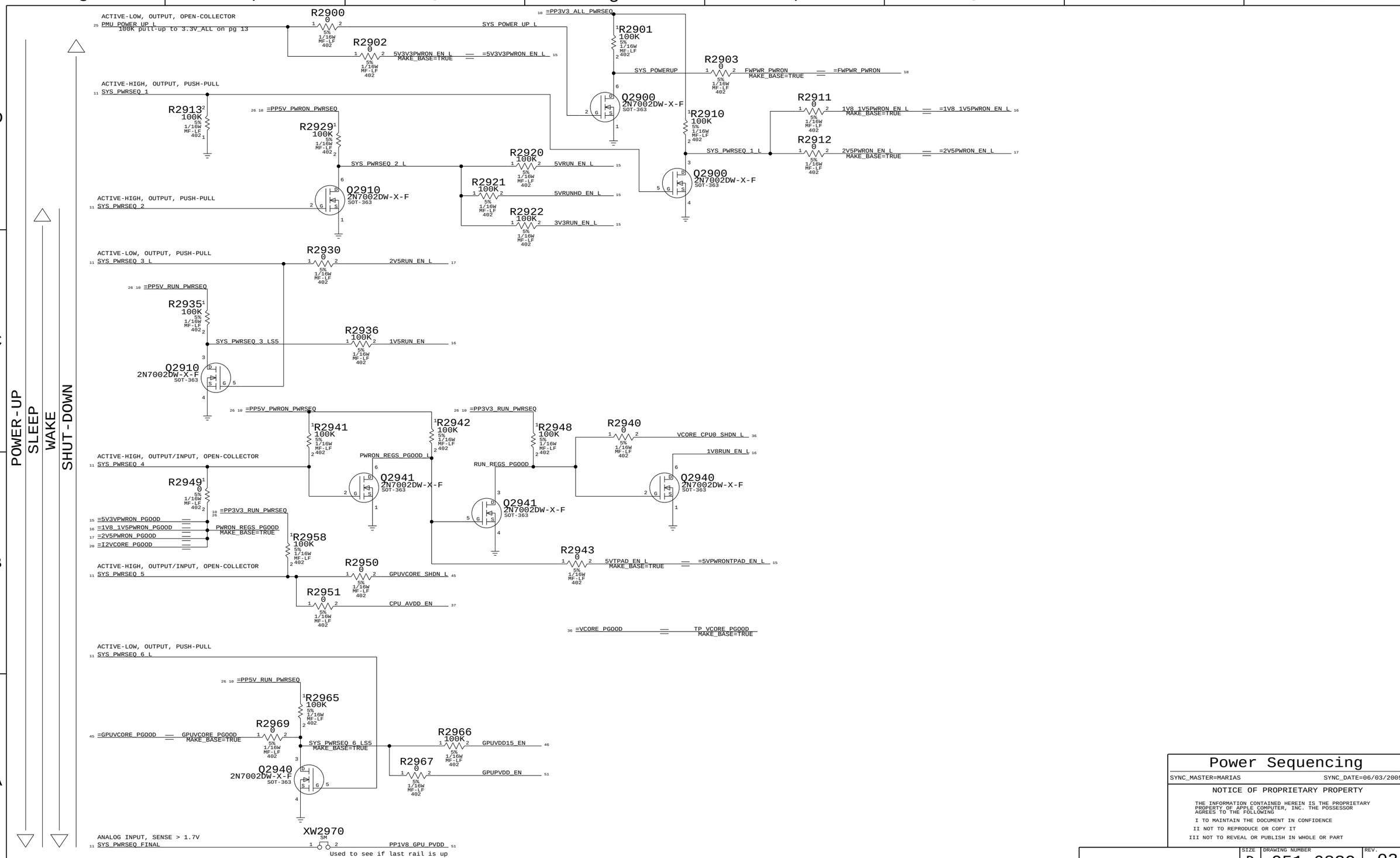

Power Sequencing

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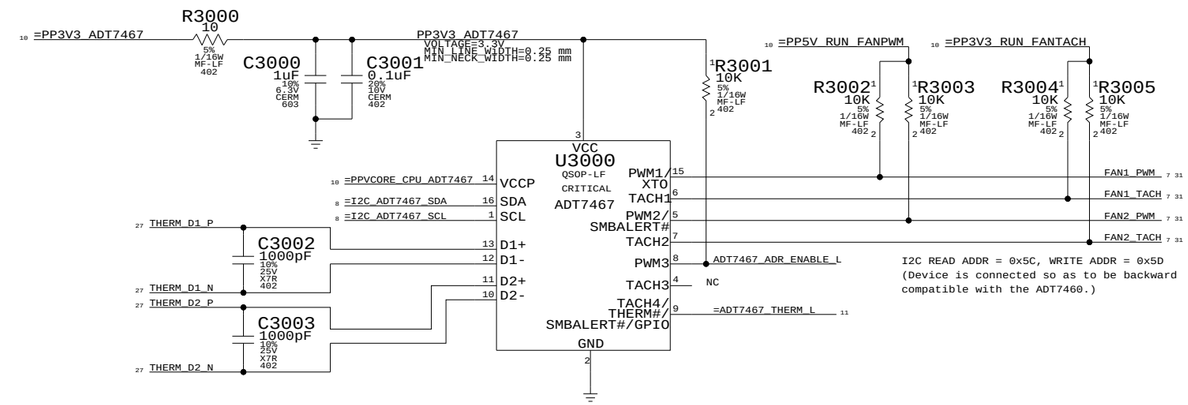
SCALE NONE	SHT 29 OF 115	

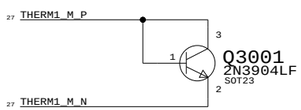
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
1528	THERM	THERM	THERM1_M	THERM1_M_P	27
1529	THERM	THERM	THERM1_M	THERM1_M_N	27
1530	THERM	THERM	THERM2_M	THERM2_M_P	27
1531	THERM	THERM	THERM2_M	THERM2_M_N	27
1532	THERM	THERM	THERM1_A	THERM1_A_P	27
1533	THERM	THERM	THERM1_A	THERM1_A_N	27
1534	THERM	THERM	THERM2_A	THERM2_A_P	27
1535	THERM	THERM	THERM2_A	THERM2_A_N	27
1536	THERM	THERM	THERM_D1	THERM_D1_P	27
1537	THERM	THERM	THERM_D1	THERM_D1_N	27
1538	THERM	THERM	THERM_D2	THERM_D2_P	27
1539	THERM	THERM	THERM_D2	THERM_D2_N	27

FAN CONTROLLER

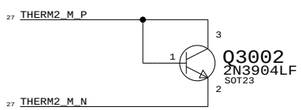


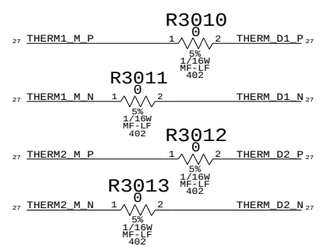
I2C READ ADDR = 0x5C, WRITE ADDR = 0x5D
(Device is connected so as to be backward compatible with the ADT7460.)

PLACE CLOSE TO CPU
MAIN1



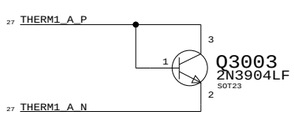
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2



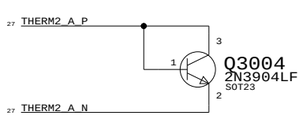


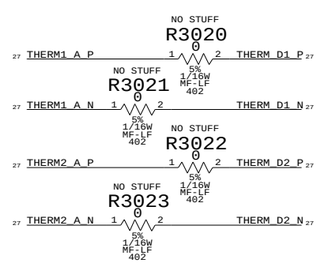
KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

PLACE UNDERNEATH UPPER RAM
ALTERNATE1



PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2





Fan Controller

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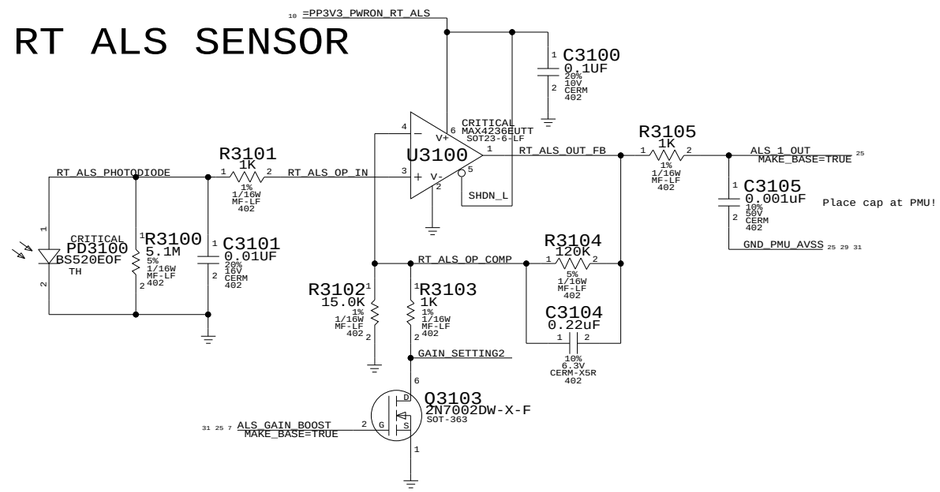
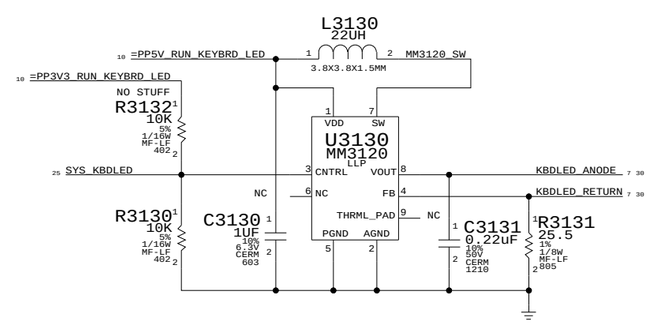
RT ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U3100	

Keyboard LED Driver



ALS Support

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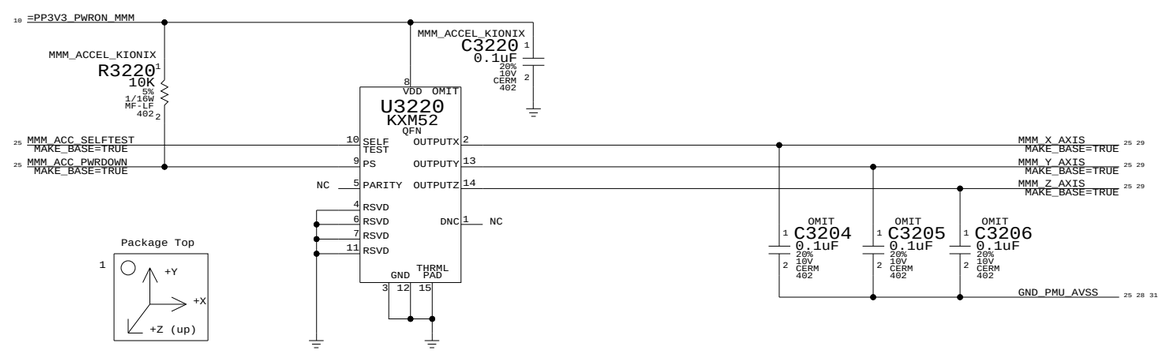
D	051-6839	02
SCALE NONE	SHT 31 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I67	THERM	THERM	
I68	THERM	THERM	
I69	THERM	THERM	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC,KIONIX,KXM52-2050,3AXIS ACCELEROMETER,SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP,CER .0047UF,10%,25V,X7R,0402,SMD	C3204,C3205,C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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APPLE COMPUTER INC.

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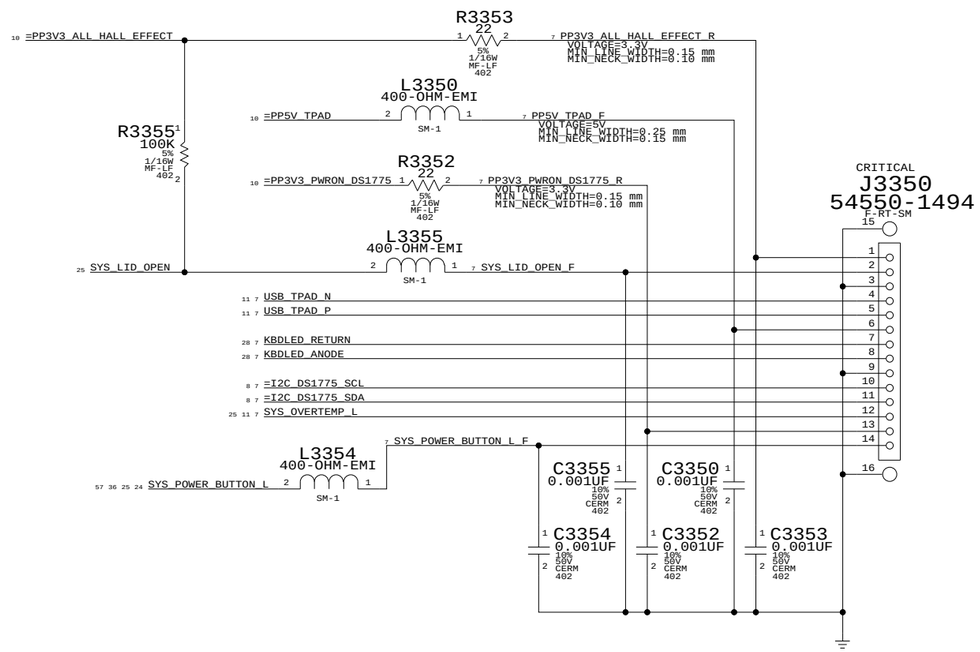
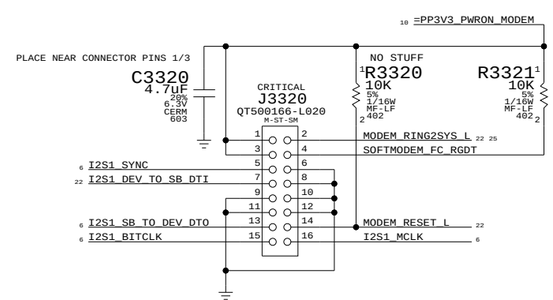
SCALE NONE SHT 32 OF 115

USB Trackpad Conn



SOFT MODEM CONN



Q41C Internal I/O I	
SYNC_MASTER=N/A	SYNC_DATE=N/A

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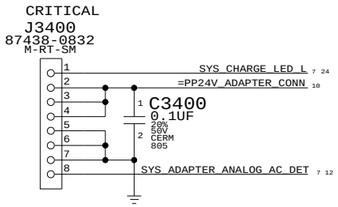
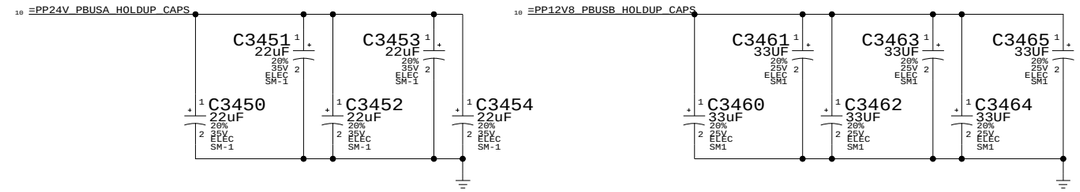
D	051-6839	02
SCALE NONE	SHT 33 OF 115	

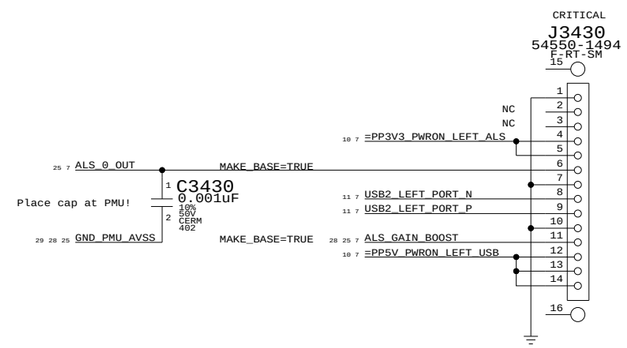
ADAPTER CONNECTOR



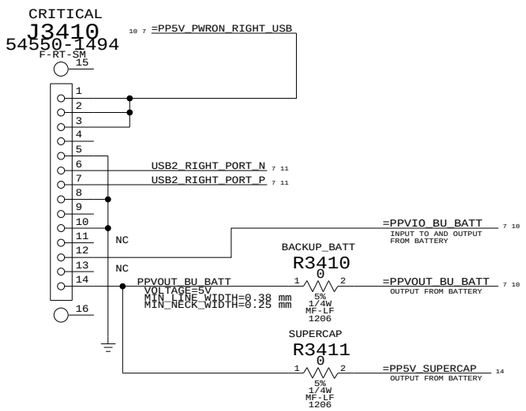
PBUS HOLD-UP CAPS



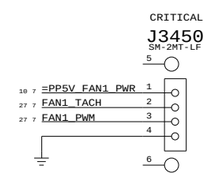
LEFT USB/LEFT ALS



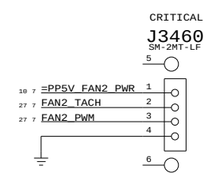
BACKUP BATTERY / RT USB CONNECTOR



CPU FAN



GPU FAN



Q41C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02

SCALE NONE SHT 34 OF 115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
MAXBUS_CLK_CPU0	CLOCK	CLOCK		MAXBUS_CLK_CPU0_R	11 32
MAXBUS_CLK_CPU1	CLOCK	CLOCK		TP_MAXBUS_CLK_CPU1_R	11 32
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_OUT_R	32
	I2_FBCLK	I2_FBCLK		I2_MAXBUS_FBCLK_OUT	21 32
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_ADDR<0..31>	9 32 33
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_DATA<0..40>	9 32 33
MAXBUS_DATA41	MAXBUS	MAXBUS		MAXBUS_DATA<41>	9 21 32 33
MAXBUS_DATA42	MAXBUS	MAXBUS		MAXBUS_DATA<42>	9 21 32 33
MAXBUS_DATA43	MAXBUS	MAXBUS		MAXBUS_DATA<43>	9 21 32 33
MAXBUS_DATA44	MAXBUS	MAXBUS		MAXBUS_DATA<44>	9 21 32 33
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_DATA<45..53>	9 32 33
MAXBUS_DATA54	MAXBUS	MAXBUS		MAXBUS_DATA<54>	9 21 32 33
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_DATA<55..61>	9 32 33
MAXBUS_DATA62	MAXBUS	MAXBUS		MAXBUS_DATA<62>	9 21 32 33
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_DATA<63>	9 32 33
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS		MAXBUS_TS_L	6 32 33
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS		MAXBUS_TA_L	6 32 33
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS		MAXBUS_TEA_L	6 32 33
MAXBUS_NB_TO_CPUS_R	MAXBUS	MAXBUS		MAXBUS_AACK_L	6 32 33
MAXBUS_CPUS_BIDIR_R	MAXBUS	MAXBUS		MAXBUS_ARTRY_L	6 32 33
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS		MAXBUS_CI_L	9 32 33
MAXBUS_DTI	MAXBUS	MAXBUS		MAXBUS_DTI<0..2>	9 32 33
MAXBUS_GBL_L	MAXBUS	MAXBUS		MAXBUS_GBL_L	9 32 33
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS		MAXBUS_TBST_L	9 32 33
MAXBUS_CPUS_TO_NBIO	MAXBUS	MAXBUS		MAXBUS_TSIZ<0..2>	9 32 33
MAXBUS_CPUS_BIDIR	MAXBUS	MAXBUS		MAXBUS_TT<0..4>	9 32 33
MAXBUS_WT_L	MAXBUS	MAXBUS		MAXBUS_WT_L	9 32 33
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS		MAXBUS_CPU0_BG_L	6 32 33
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS		MAXBUS_CPU0_BR_L	6 32 33
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS		MAXBUS_CPU0_DBG_L	6 32 33
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS		MAXBUS_CPU0_DRDY_L	6 32 33
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS		MAXBUS_CPU0_HIT_L	6 32 33
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS		MAXBUS_CPU1_BG_L	6 32
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS		MAXBUS_CPU1_BR_L	6 32
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS		MAXBUS_CPU1_DBG_L	6 32
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS		MAXBUS_CPU1_DRDY_L	6 32
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS		MAXBUS_CPU1_HIT_L	6 32

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_I2_MAXBUS

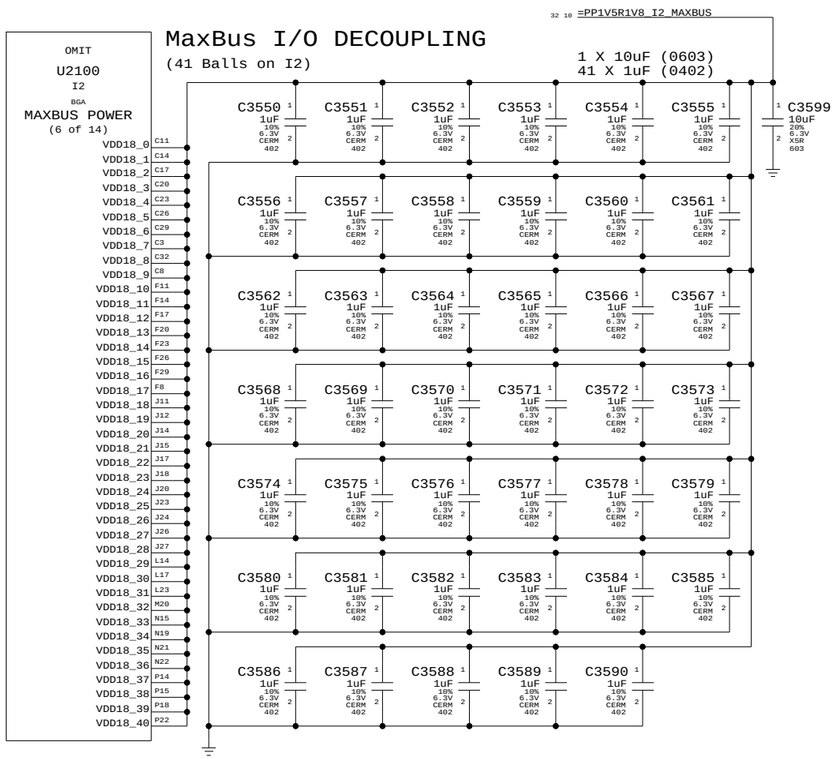
BOM options provided by this page:
- MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

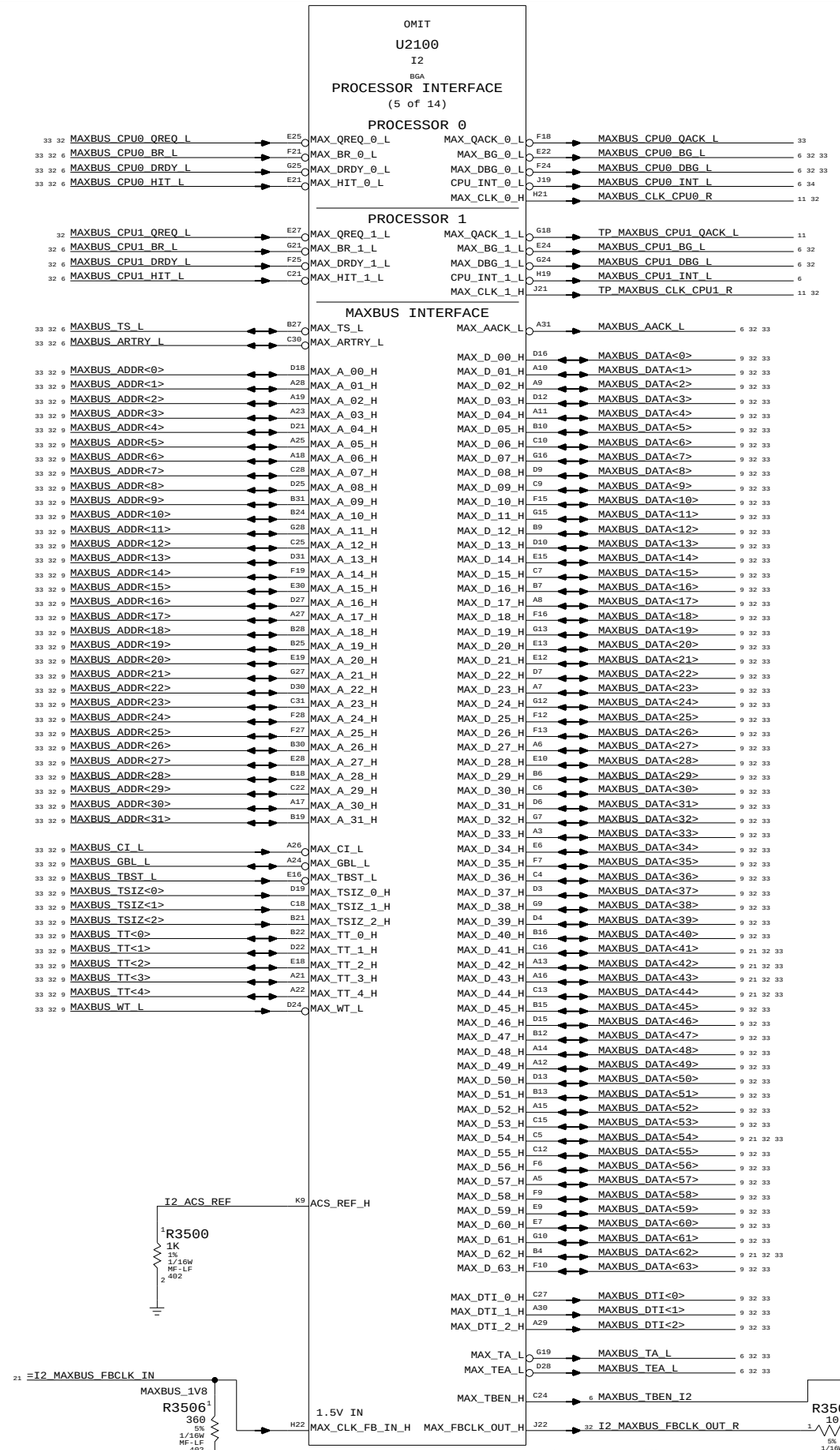
Signal aliases required by this page:
- =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING

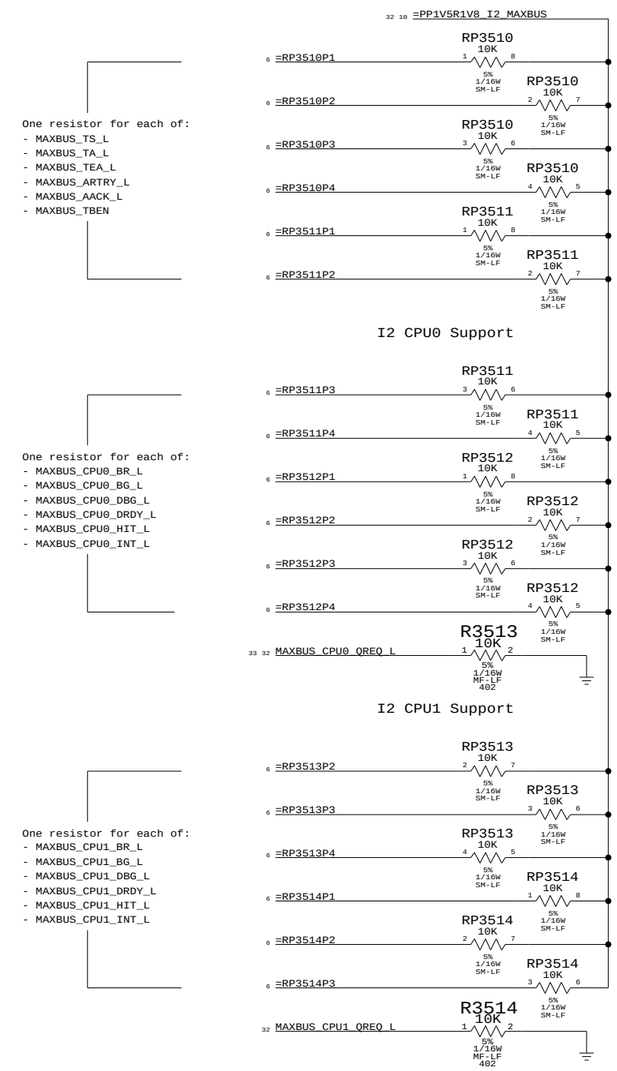
(41 Balls on I2)

1 X 10uF (0603)
41 X 1uF (0402)





MaxBus Pull-ups / Pull-downs



I2 Processor Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE NONE	SHT 35 OF 115	

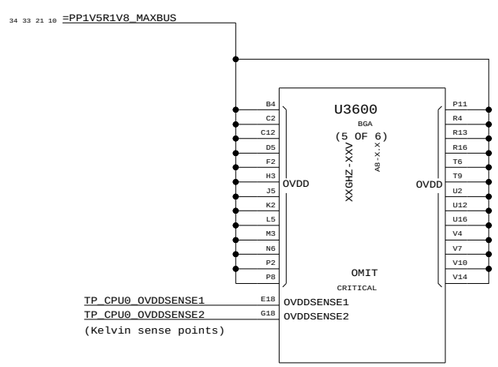
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR
=MAXBUS_CPU0_CLK	CLOCK	CLOCK	

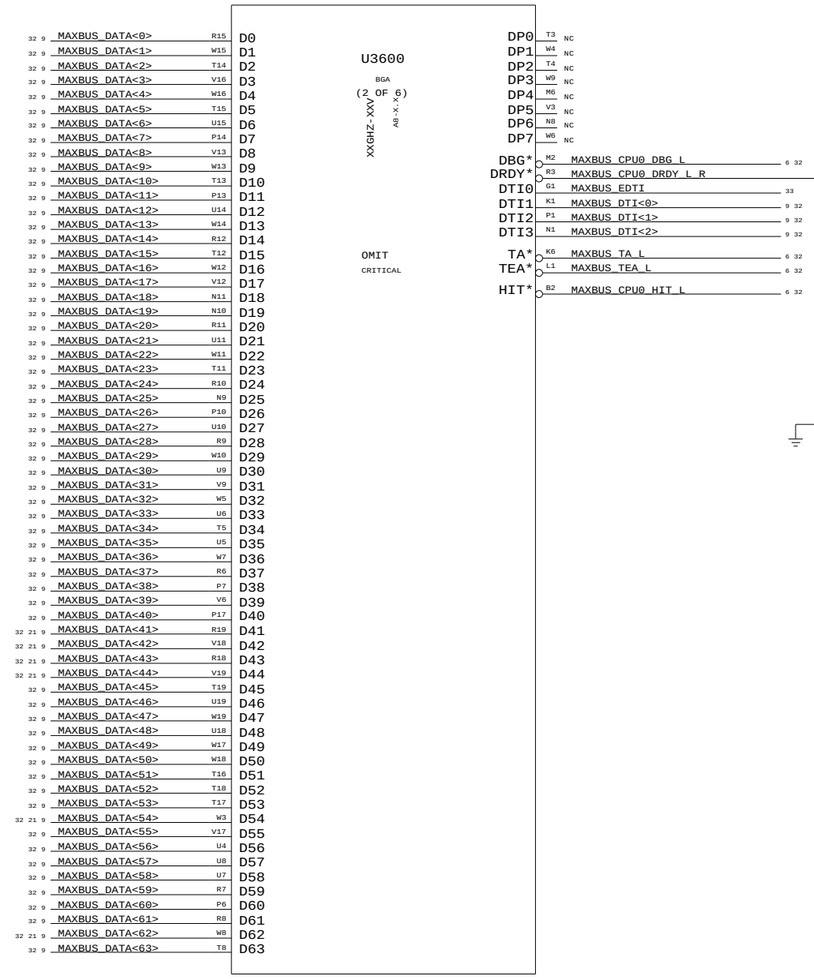
Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS

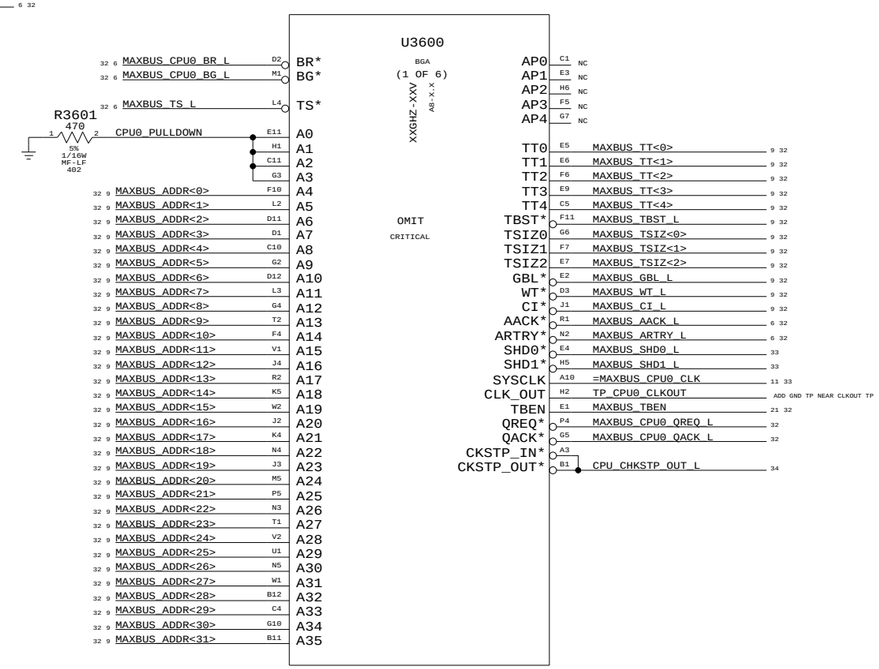
Signal aliases required by this page:
- =MAXBUS_CPU0_CLK

BOM options provided by this page:
(NONE)





R3600
0
5%
1/10W
MF-LF
402
PLACE RC GLITCH FILTER
CLOSE TO CPU PIN
MAXBUS_CPU0_DRDY_L
C3600
10PF
5%
50V
CERM
402

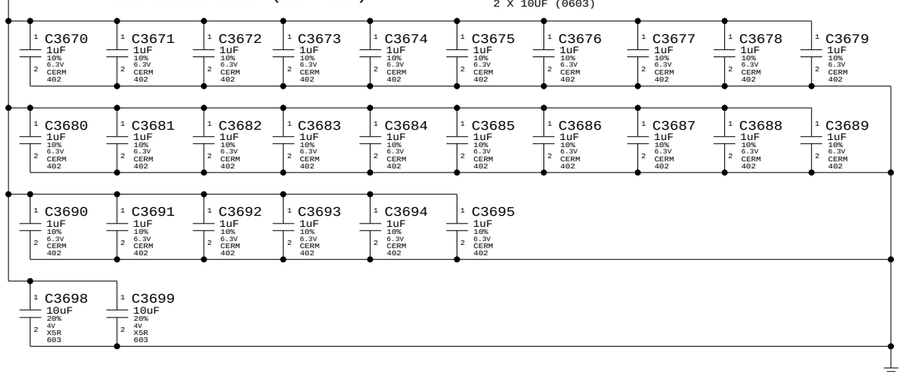


R3601
470
5%
1/10W
MF-LF
402

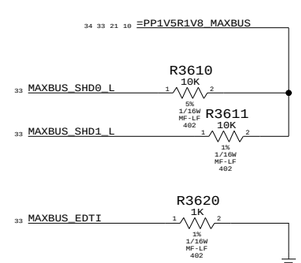
=PP1V5R1V8_MAXBUS

VIO DECOUPLING (28 PINS)

26 X 1UF (0402)
2 X 10UF (0603)



MAXBUS Straps



A8 MaxBus (CPU0)	
SYNC_MASTER=MARIAS	SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 36 OF 115	

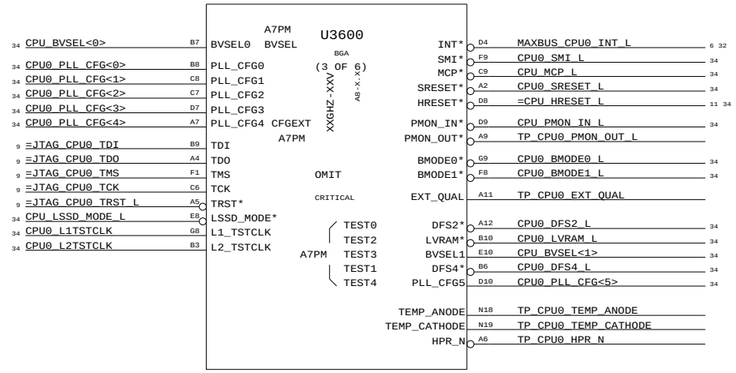
Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSEL

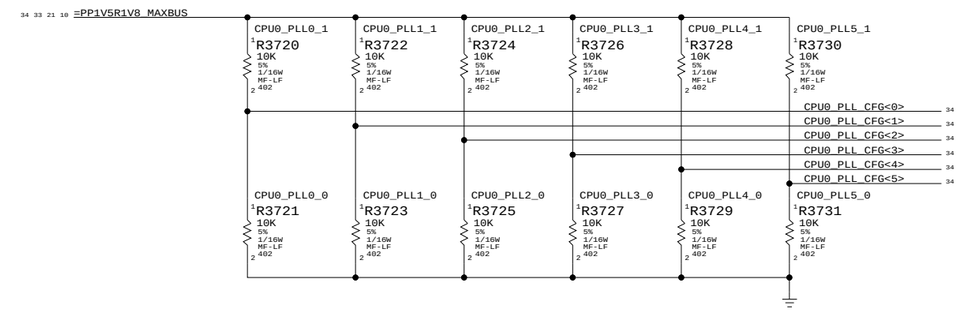
Signal aliases required by this page:
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
  One of these must be selected to set the Maxbus voltage
  * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
  One of these must be selected to ensure the the above strap is interpreted correctly



CPU0 PLL CONFIG CIRCUITRY



BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE

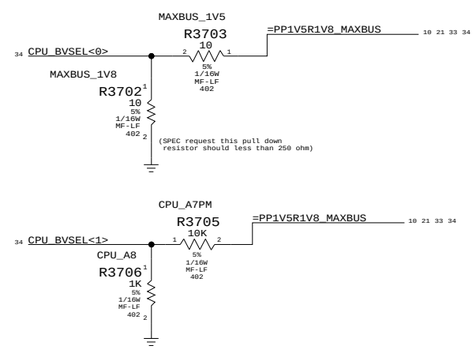
A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

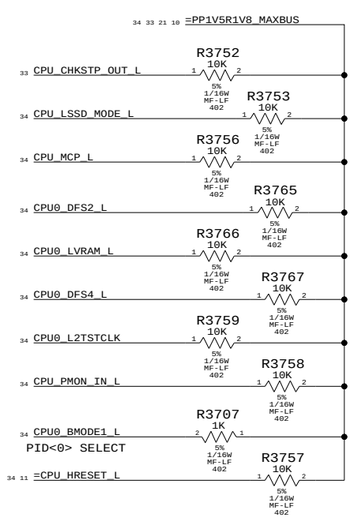
A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

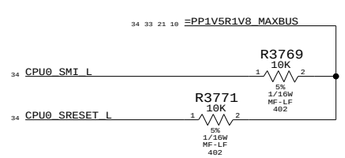
MAXBUS VSEL



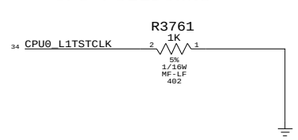
CPU PULLUPS



INTERRUPT PULL-UPS



CPU PULLDOWNS



CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT F/2	DFS SUPPORT F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

A8 Configuration Straps

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02

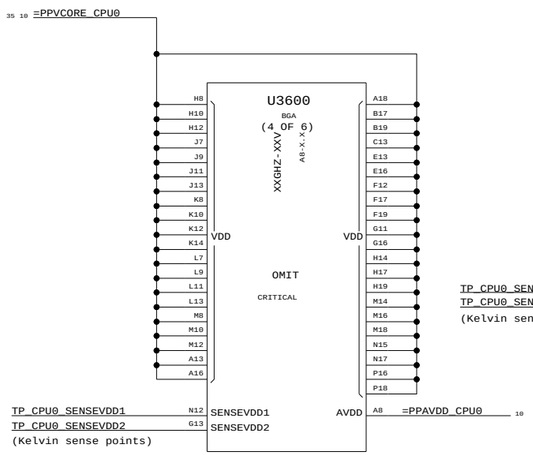
SCALE NONE SHT 37 OF 115

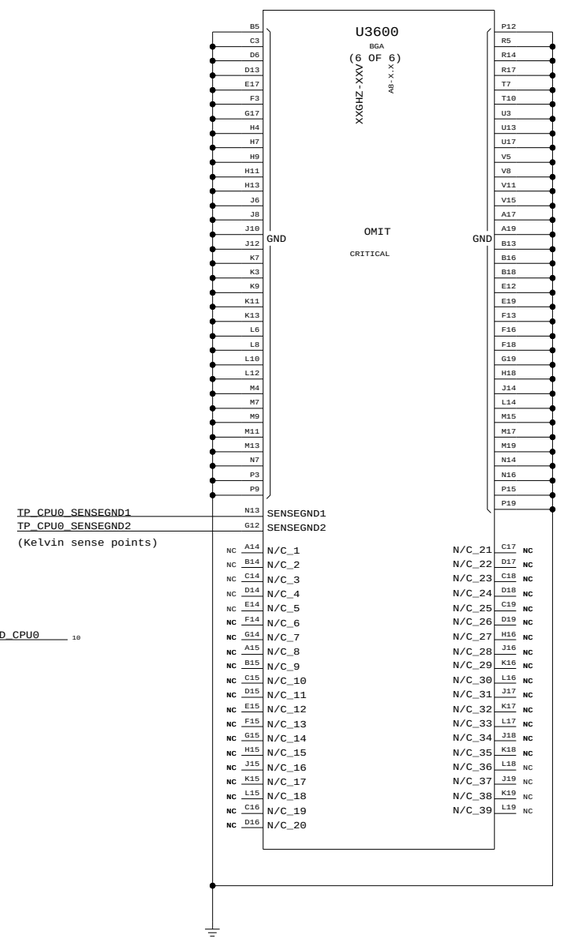
Page Notes

Power aliases required by this page:
- =PPVCORE_CPU0

Signal aliases required by this page:
(NONE)

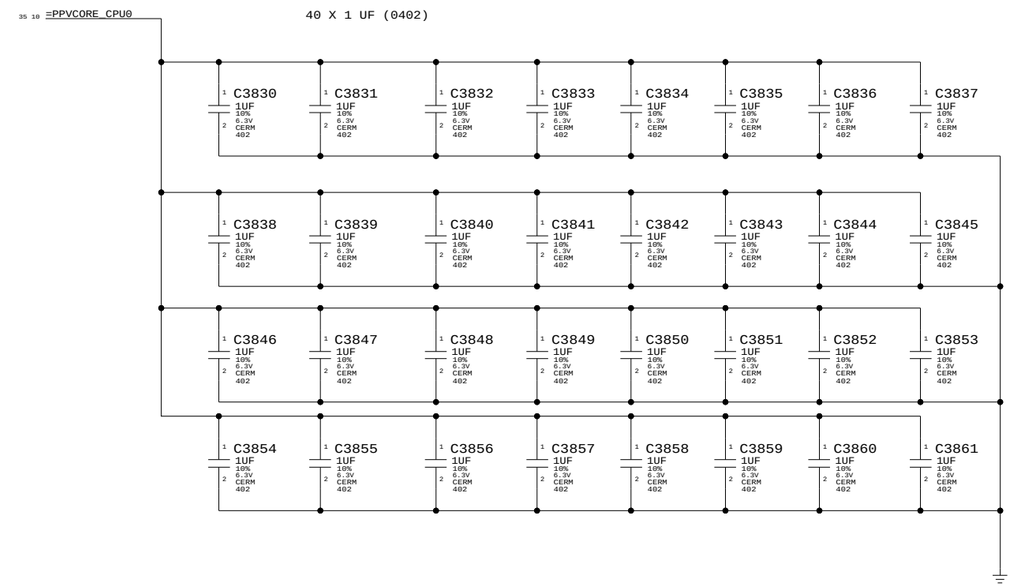
BOM options provided by this page:
(NONE)



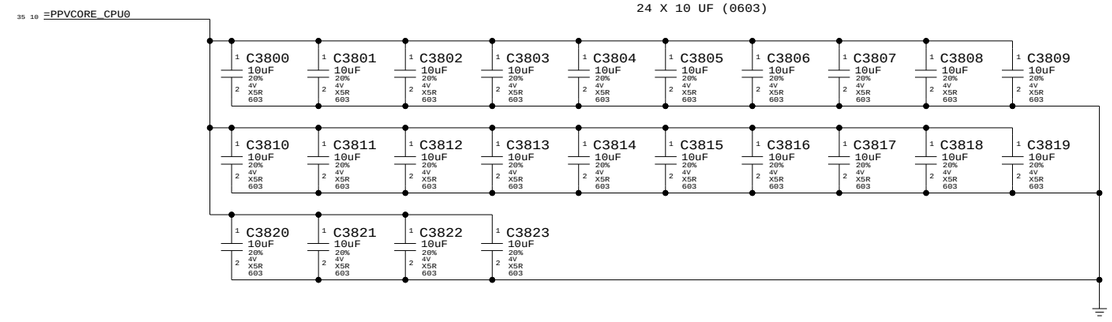


VCORE BULK CAPS

40 X 1 UF (0402)



24 X 10 UF (0603)



A8 Power (CPU0)

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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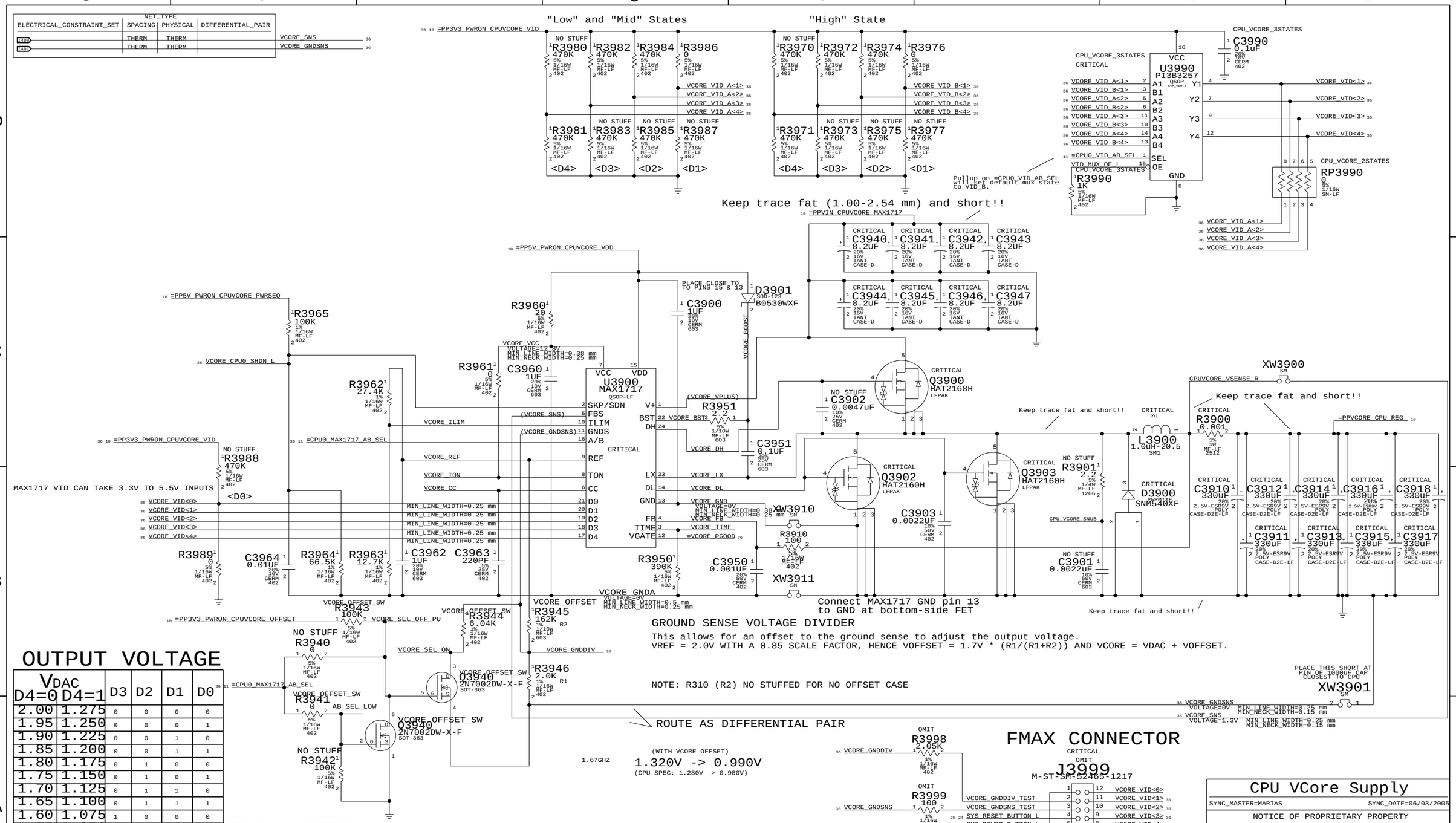
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 38 OF 115	


"Low" and "Mid" States
"High" State
Keep trace fat (1.00-2.54 mm) and short!!
Keep trace fat and short!!
Pullup on =CPU0_VID_AB_SEL will set default mux state to VID_B.
MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS
Connect MAX1717 GND pin 13 to GND at bottom-side FET
GROUND SENSE VOLTAGE DIVIDER
This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.
NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE
ROUTE AS DIFFERENTIAL PAIR
(WITH VCORE OFFSET)
1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)
1.67GHZ
FMAX CONNECTOR
FOR V-STEP:
When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1
If all pull-ups are >=100K and all pull-downs are <=1K, V_A = V_B .
OUTPUT VOLTAGE
CPU VCore Supply
SYNC_MASTER=MARIAS
SYNC_DATE=06/03/2005
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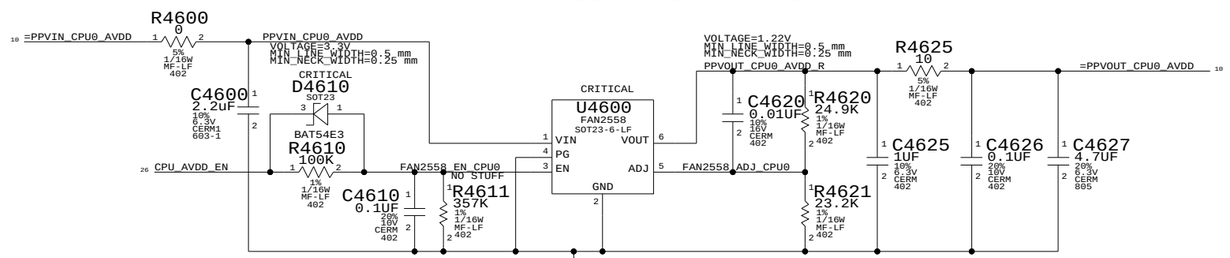
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6839
REV. 02
SCALE NONE
SHT 39 OF 115

CPU PLL POWER SUPPLY



AVDD=0.59*(1+R4620/4621)

CPU AVDD Supply

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 46 OF 115	

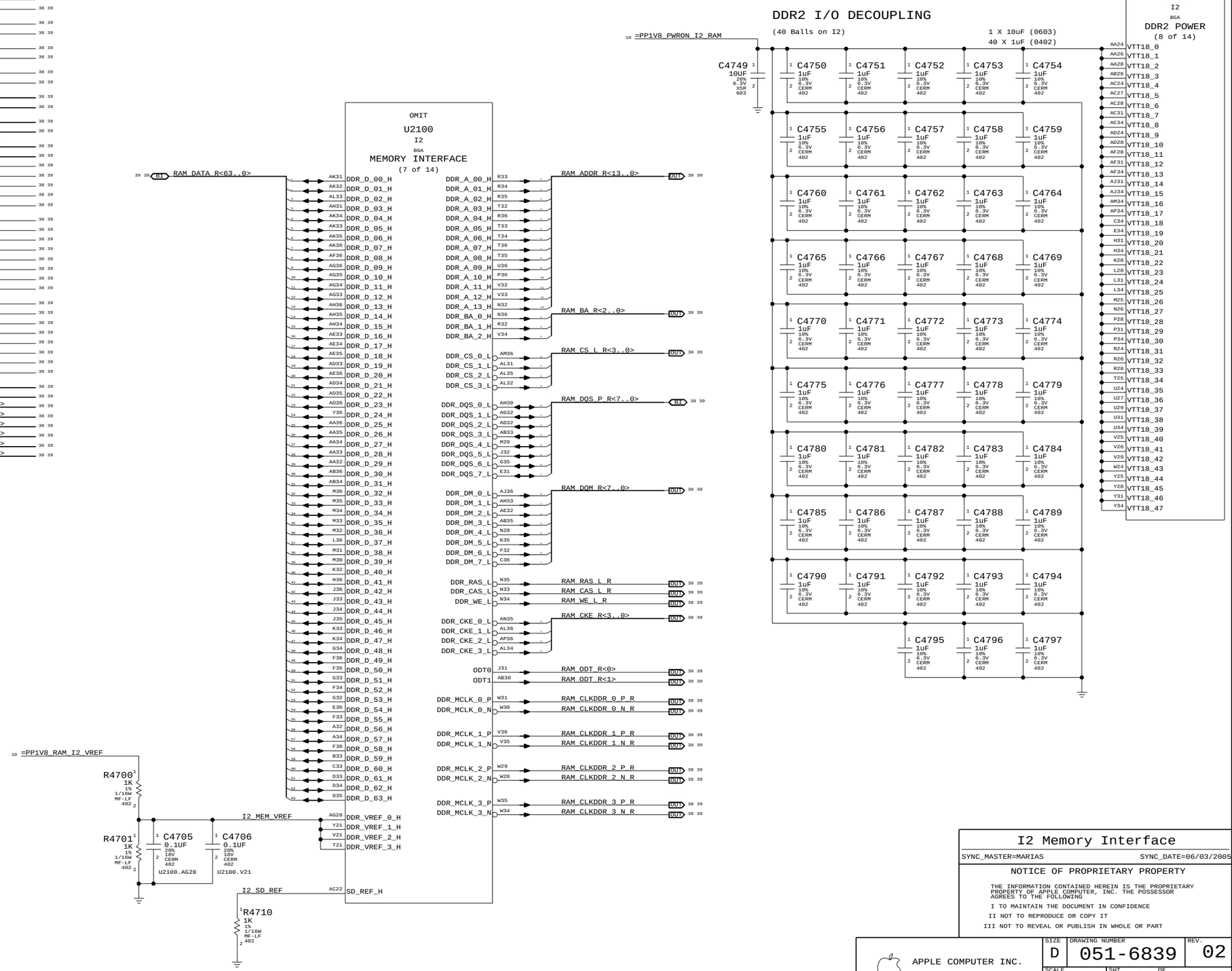
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R	38 39
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R	38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R	38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R	38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R	38 39
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0>	38 39
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2>	38 39
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0>	38 39
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0>	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_RAS_L_R	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R	38 39
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R	38 39
RAM_ODT0	RAM	RAM		RAM_ODT_R<0>	38 39
RAM_ODT1	RAM	RAM		RAM_ODT_R<1>	38 39
RAM_DQS0	RAM	RAM		RAM_DQS_P_R<0>	38 39
RAM_DQS1	RAM	RAM		RAM_DQS_P_R<1>	38 39
RAM_DQS2	RAM	RAM		RAM_DQS_P_R<2>	38 39
RAM_DQS3	RAM	RAM		RAM_DQS_P_R<3>	38 39
RAM_DQS4	RAM	RAM		RAM_DQS_P_R<4>	38 39
RAM_DQS5	RAM	RAM		RAM_DQS_P_R<5>	38 39
RAM_DQS6	RAM	RAM		RAM_DQS_P_R<6>	38 39
RAM_DQS7	RAM	RAM		RAM_DQS_P_R<7>	38 39
RAM_DQM0	RAM	RAM		RAM_DQM_R<0>	38 39
RAM_DQM1	RAM	RAM		RAM_DQM_R<1>	38 39
RAM_DQM2	RAM	RAM		RAM_DQM_R<2>	38 39
RAM_DQM3	RAM	RAM		RAM_DQM_R<3>	38 39
RAM_DQM4	RAM	RAM		RAM_DQM_R<4>	38 39
RAM_DQM5	RAM	RAM		RAM_DQM_R<5>	38 39
RAM_DQM6	RAM	RAM		RAM_DQM_R<6>	38 39
RAM_DQM7	RAM	RAM		RAM_DQM_R<7>	38 39
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0>	38 39
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8>	38 39
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16>	38 39
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24>	38 39
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32>	38 39
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40>	38 39
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48>	38 39
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56>	38 39

Page Notes

Power aliases required by this page:
- =PP1V8_PWRON_I2_RAM
- =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 Memory Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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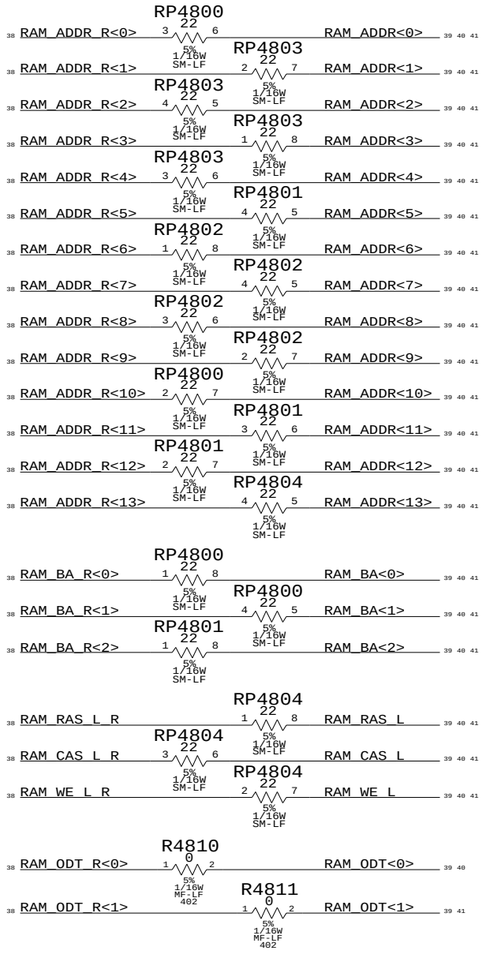
SCALE NONE SHT 47 OF 115

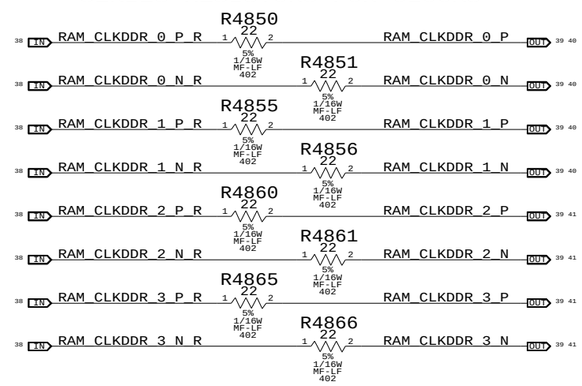
Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

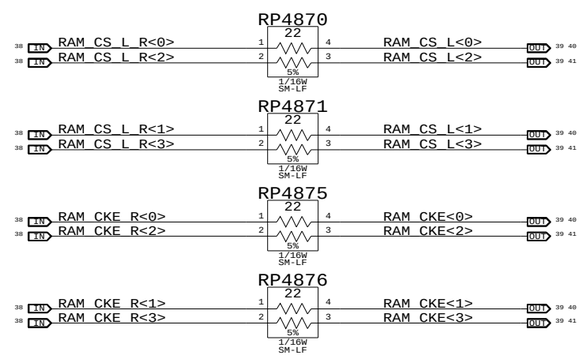


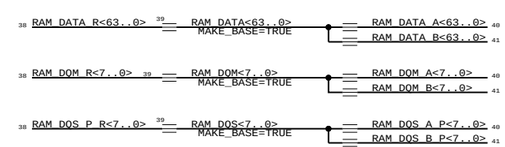
SERIES RESISTORS FOR CLOCKS

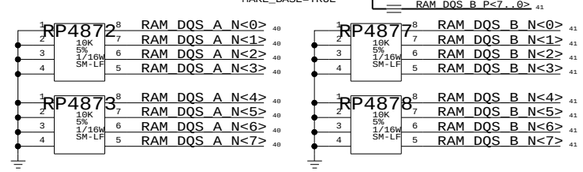


SERIES RESISTORS FOR CS / CKE

Do not swap with other RPAKs







ECSETs provided by memory controller.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	NET_TYPE DIFFERENTIAL_PAIR	
I189	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P
I190	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N
I192	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P
I193	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N
I197	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P
I199	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N
I198	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P
I200	RAM_DIFF	RAM_DIFF	RAM_CLK_4	RAM_CLKDDR_3_N
I205	RAM	RAM		RAM_CKE<3..0>
I204	RAM	RAM		RAM_CS_L<3..0>
I203	RAM	RAM		RAM_ADDR<13..0>
I202	RAM	RAM		RAM_BA<2..0>
I201	RAM	RAM		RAM_RAS_L
I208	RAM	RAM		RAM_CAS_L
I207	RAM	RAM		RAM_WE_L
I209	RAM	RAM		RAM_ODT<1..0>
I206	RAM	RAM		RAM_DQS<7..0>
I208	RAM	RAM		RAM_DOM<7..0>
I210	RAM	RAM		RAM_DATA<63..0>

Memory Series Termination

SYNC_MASTER=MARIAS-NDIFF SYNC_DATE=N/A

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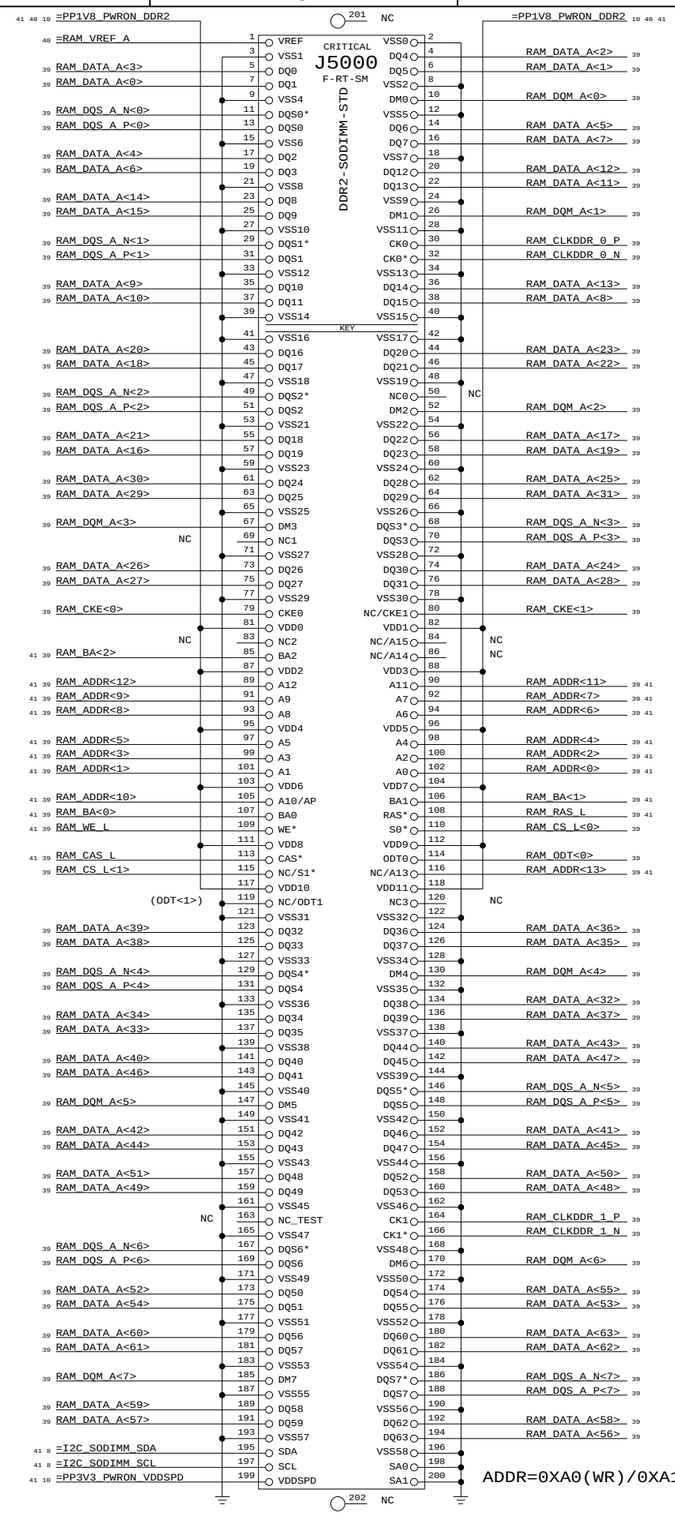
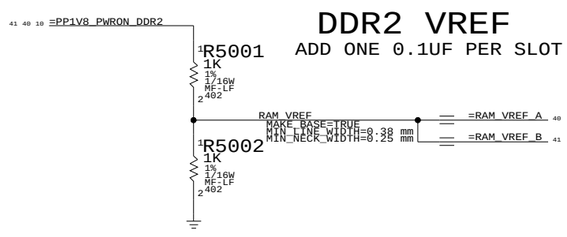
D	051-6839	02

SCALE NONE SHT 48 OF 115

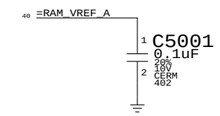


SLOT "A"
UPPER/STD SLOT
FACTORY SLOT

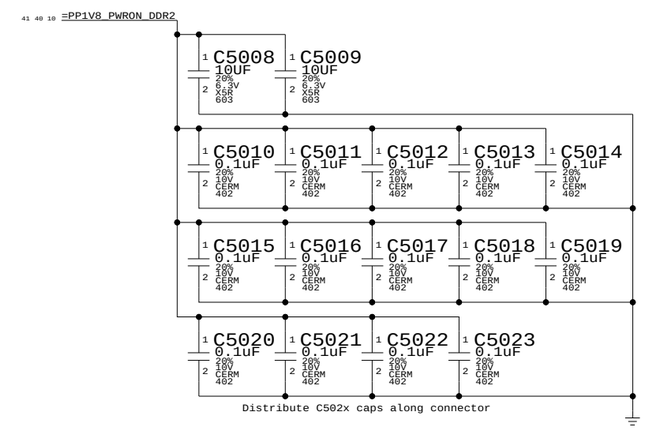
DDR2 VREF
ADD ONE 0.1UF PER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "A"



Distribute C502x caps along connector

DDR2 SO-DIMM Slot A

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
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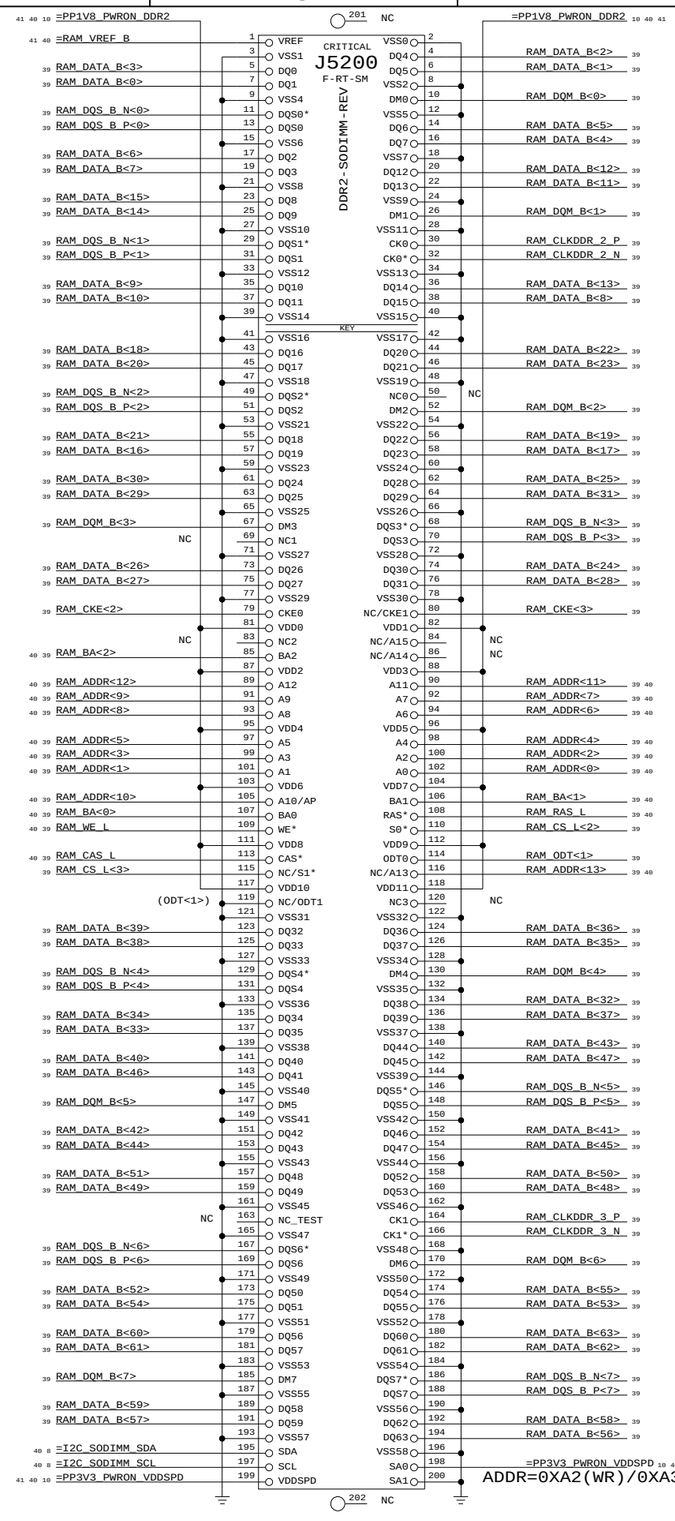
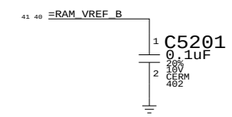
SCALE NONE	SHT 50 OF 115	

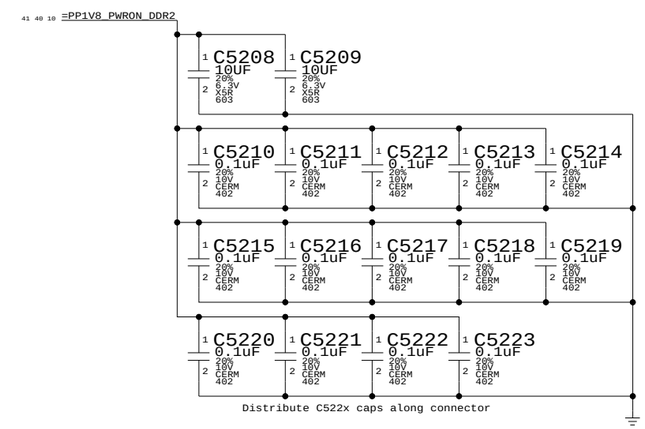
SLOT "B"
LOWER/REV SLOT
CUSTOMER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 52 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R	48
FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0>	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0>	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R	48
FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R	48
FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0>	48
FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1>	48
FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2>	48
FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3>	48
FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4>	48
FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5>	48
FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6>	48
FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7>	48
FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0>	48
FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1>	48
FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2>	48
FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3>	48
FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4>	48
FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5>	48
FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6>	48
FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7>	48
FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0>	48
FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8>	48
FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16>	48
FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24>	48
FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32>	48
FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40>	48
FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48>	48
FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56>	48

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R	48
FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R	48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0>	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0>	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R	48
FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R	48
FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0>	48
FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1>	48
FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2>	48
FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3>	48
FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4>	48
FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5>	48
FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6>	48
FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7>	48
FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0>	48
FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1>	48
FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2>	48
FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3>	48
FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4>	48
FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5>	48
FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6>	48
FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7>	48
FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0>	48
FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8>	48
FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16>	48
FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24>	48
FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32>	48
FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40>	48
FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48>	48
FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56>	48

M11 Frame Buffer Constraints

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
AGP_CLK	CLOCK	CLOCK		AGP_CLK66M_GPU_R 11 43
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT_R 43
	I2_FBCLK	I2_FBCLK		I2_AGP_FBCLK_OUT 21 43
AGP_AD_0	AGP	AGP		AGP_AD<15..0> 43 44
AGP_AD_1	AGP	AGP		AGP_AD<31..16> 43 44
AGP_AD_0	AGP	AGP		AGP_CBE_L<1..0> 43 44
AGP_AD_1	AGP	AGP		AGP_CBE_L<3..2> 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_P 43 44
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0	AGP_AD_STB0_N 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_P 43 44
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1	AGP_AD_STB1_N 43 44
AGP_SBA	AGP	AGP		AGP_SBA<7..0> 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_P 43 44
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB	AGP_SB_STB_N 43 44
AGP_ST	AGP	AGP		AGP_ST<3..0> 43 44
AGP_CTL	AGP	AGP		AGP_FRAME_L 6 43 44
AGP_CTL	AGP	AGP		AGP_DEVSEL_L 6 43 44
AGP_CTL	AGP	AGP		AGP_IRDY_L 6 43 44
AGP_CTL	AGP	AGP		AGP_TRDY_L 6 43 44
AGP_CTL	AGP	AGP		AGP_STOP_L 6 43 44
AGP_PAR	AGP	AGP		AGP_PAR 43 44
AGP_DEV_CTL	AGP	AGP		AGP_PIPE_L 43
AGP_DEV_CTL	AGP	AGP		AGP_WBF_L 43 44
AGP_DEV_CTL	AGP	AGP		AGP_RBF_L 6 43 44
	AGP	AGP		AGP_REQ_L 6 43 44
	AGP	AGP		AGP_GNT_L 6 43 44

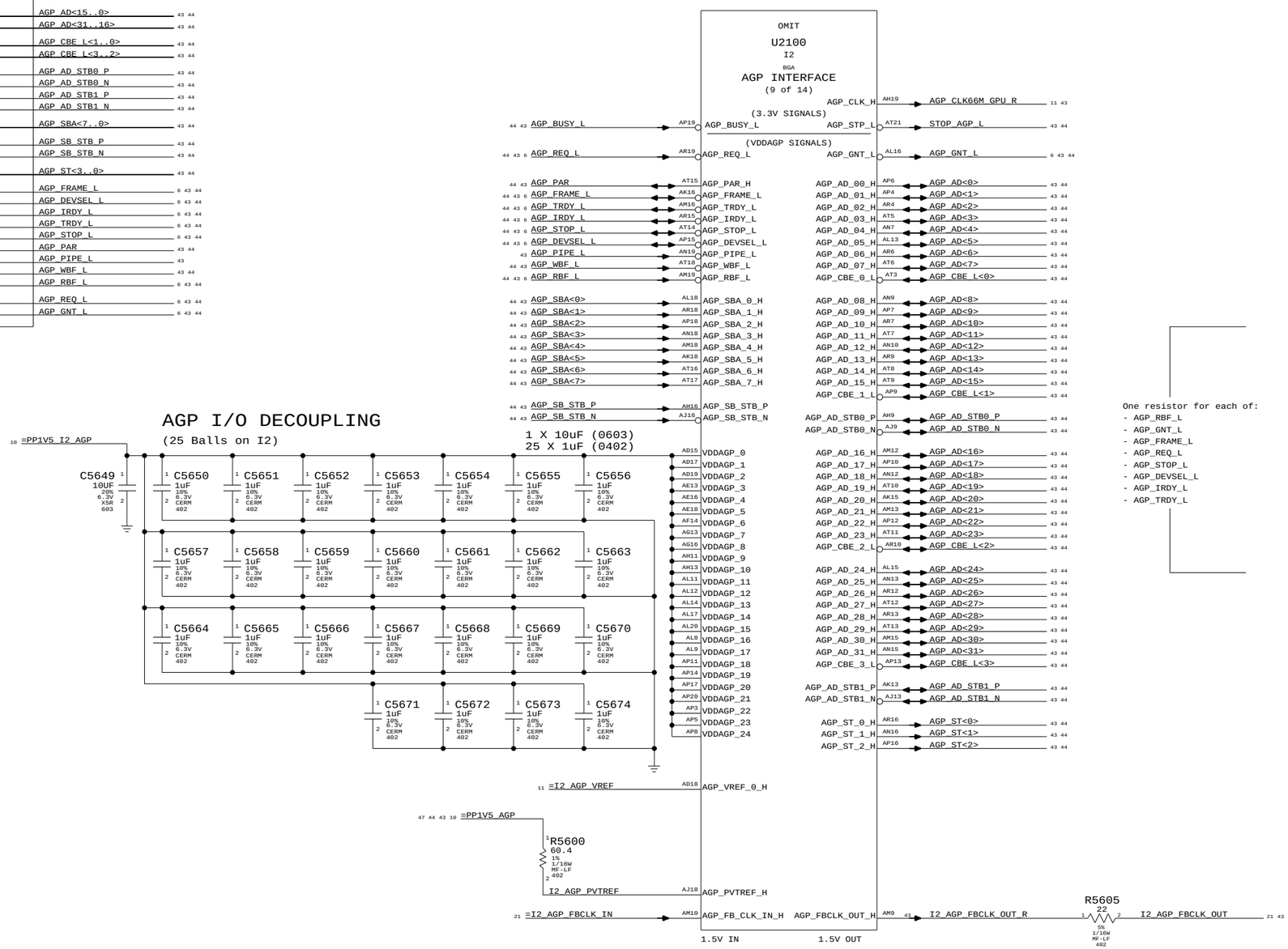
Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP
- =PP1V5_I2_AGP

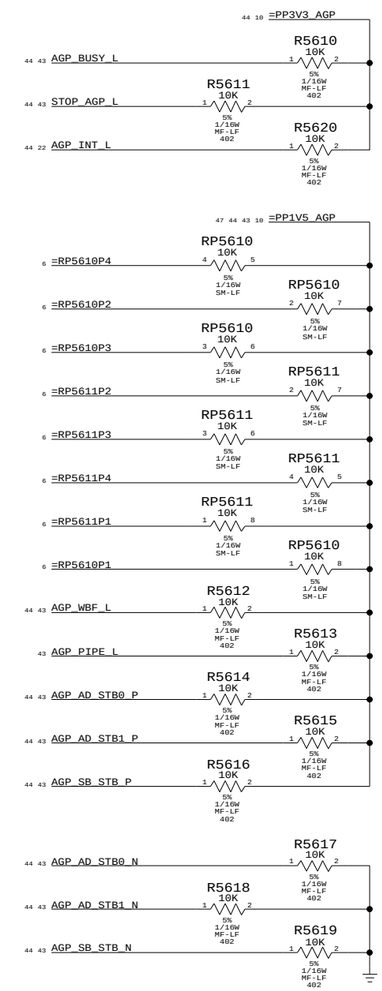
Signal aliases required by this page:
- =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
- =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
(NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.



AGP PULL-UPS/PULL DOWNS



One resistor for each of:
- AGP_RBF_L
- AGP_GNT_L
- AGP_FRAME_L
- AGP_REQ_L
- AGP_STOP_L
- AGP_DEVSEL_L
- AGP_IRDY_L
- AGP_TRDY_L

I2 AGP Interface

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
LT98	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

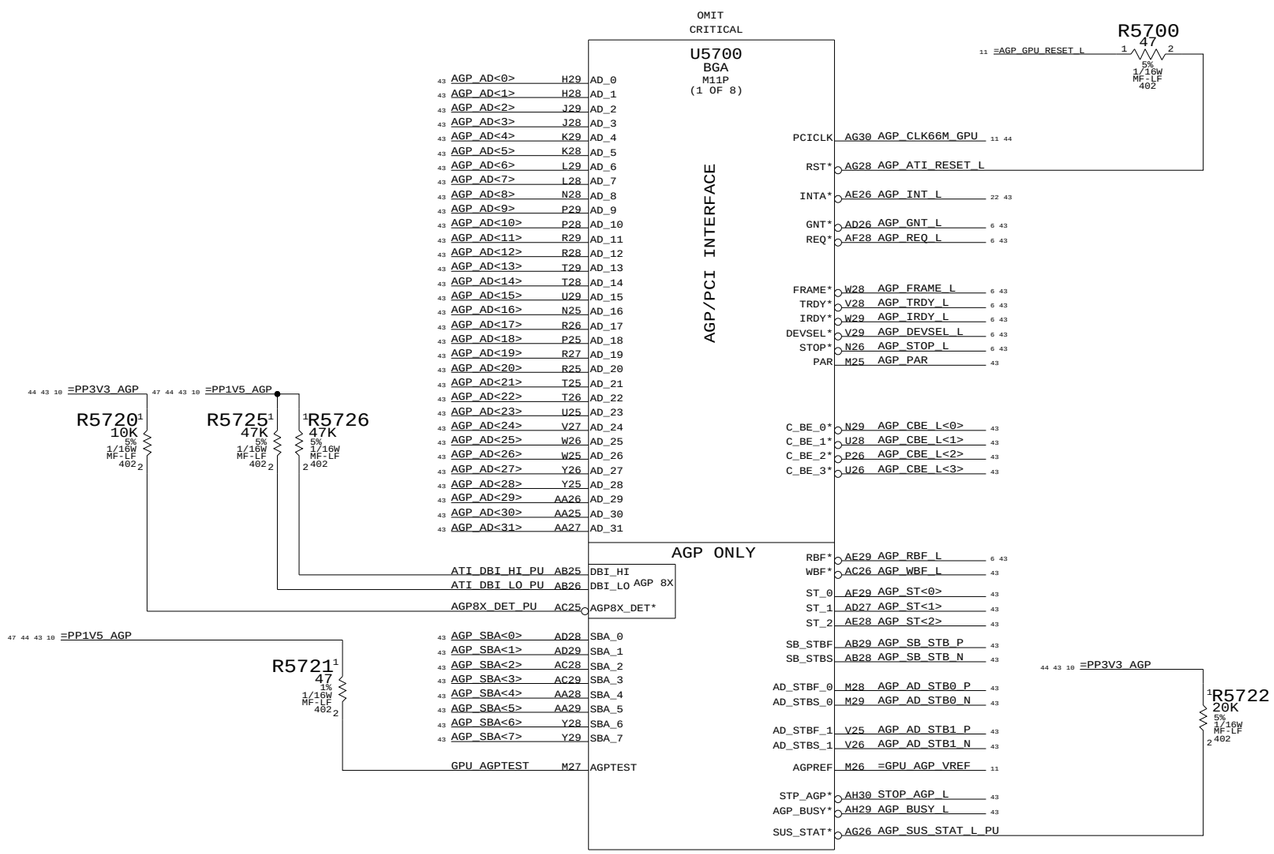
Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP

Signal aliases required by this page:
- =AGP_VREF - VRef divider output for both GPU and NB
- =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
(NONE)

NOTE: AGP 8x signals are not provided by this page.



GPU (M11) AGP Interface

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SIZE	DRAWING NUMBER	REV.
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Page Notes

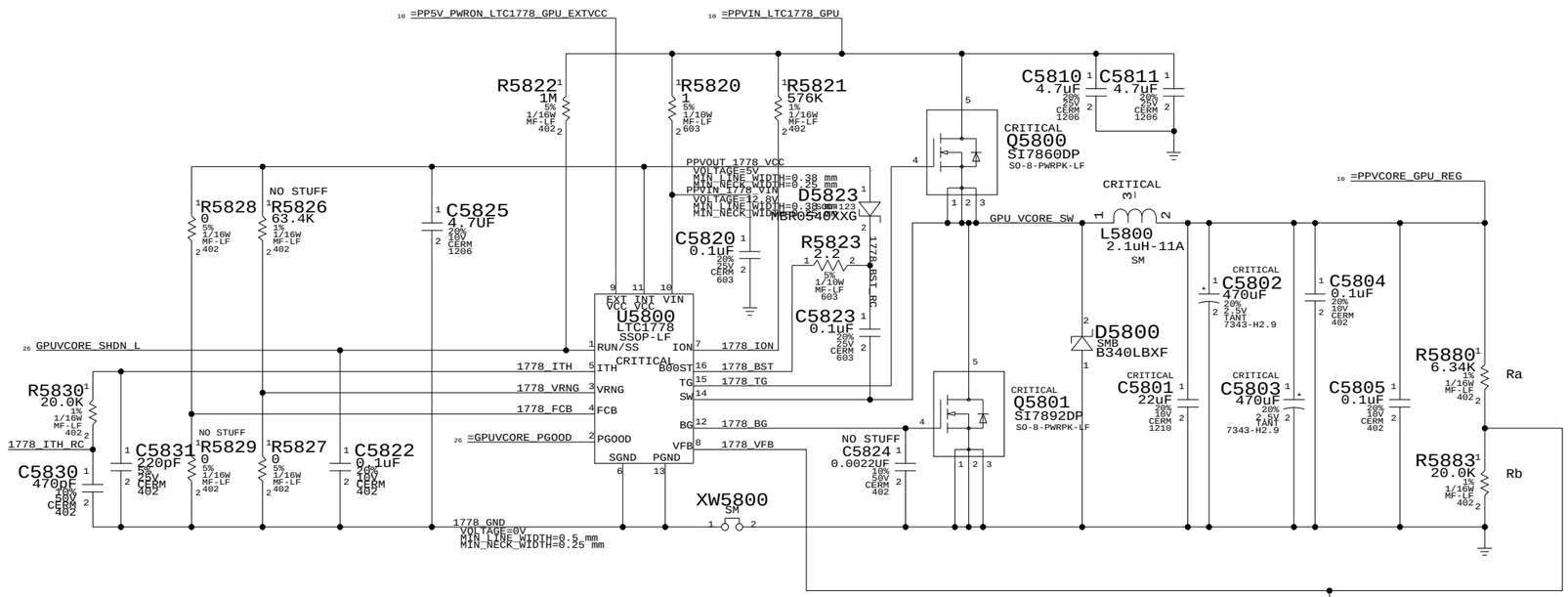
Power aliases required by this page:
- =PPVIN_LTC1778_GPU
- =PP5V_PWRON_LTC1778_GPU_EXTVCC
- =PPVCORE_GPU_REG

Signal aliases required by this page:
- =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
- GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCORE SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))

WHEN VCORE_CNTL LOW => 1.054V
1.054V = 0.8V * (1 + Ra / Rb)

GPU VCore Supply

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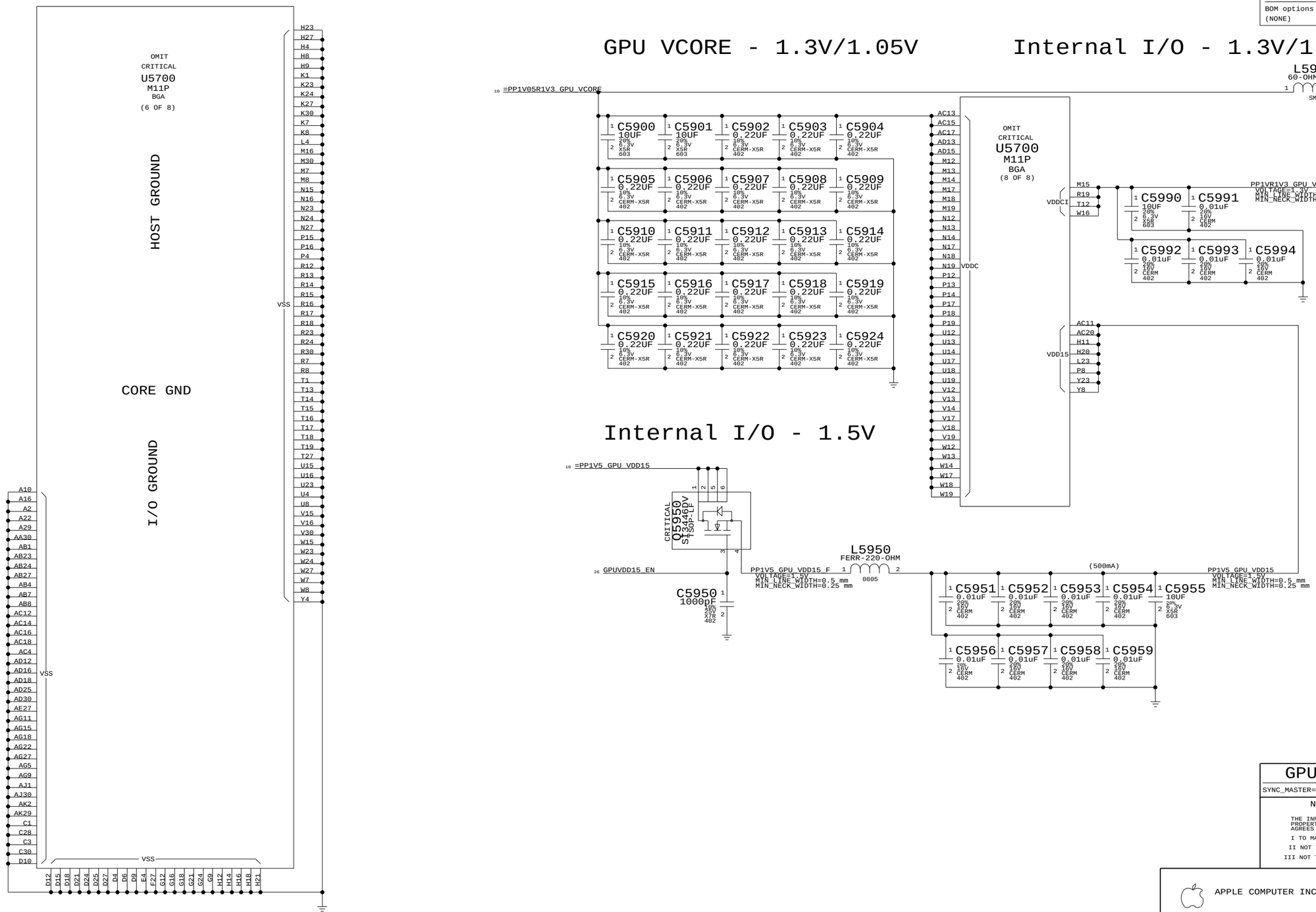
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GPU (M11) Core Power

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE

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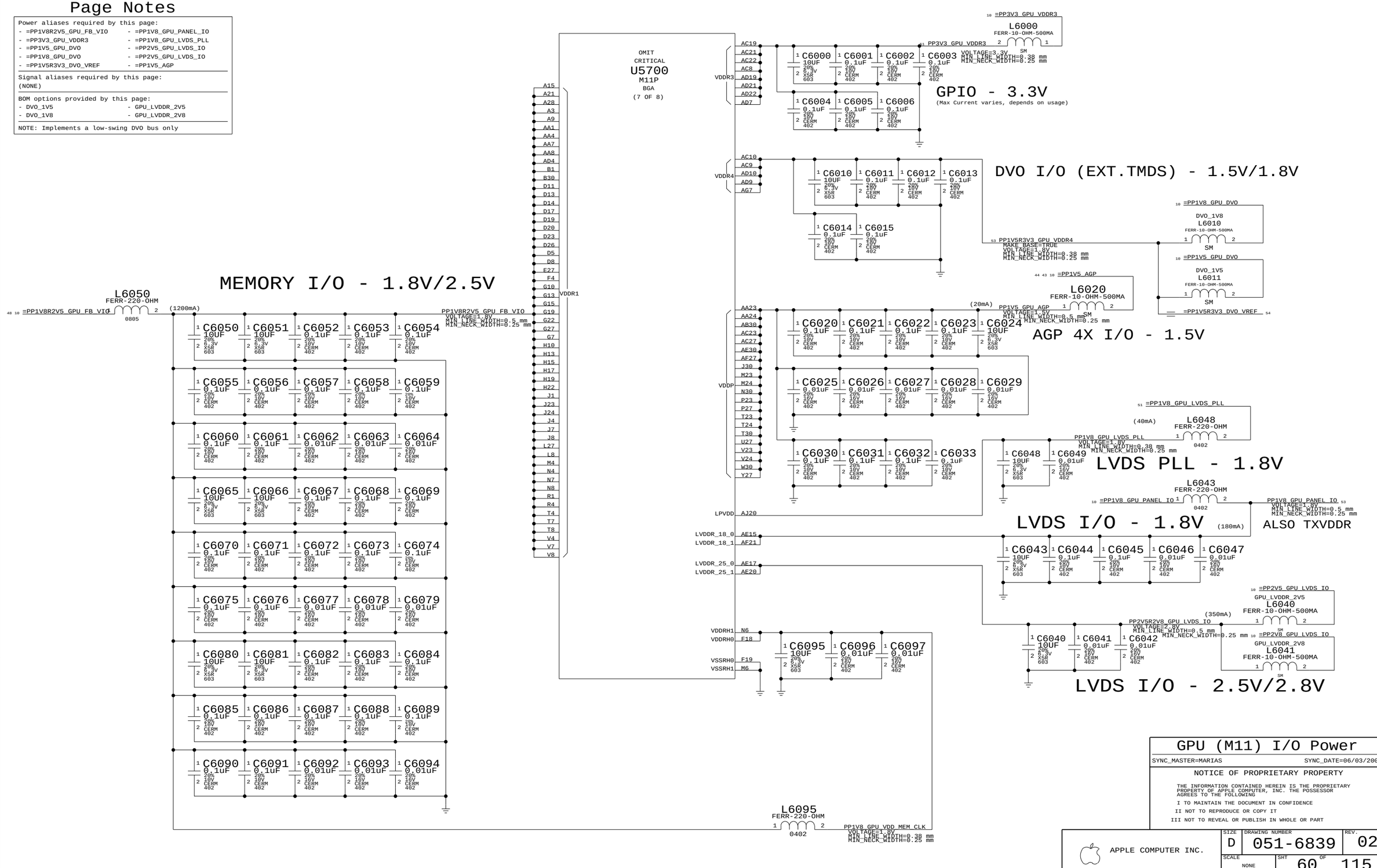
Page Notes

Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP3V3_GPU_VDDR3
- =PP1V5_GPU_DVO
- =PP1V8_GPU_DVO
- =PP1V5R3V3_DVO_VREF
- =PP1V8_GPU_PANEL_IO
- =PP1V8_GPU_LVDS_PLL
- =PP2V5_GPU_LVDS_IO
- =PP2V5_GPU_LVDS_IO
- =PP1V5_AGP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- DVO_1V8
- GPU_LVDDR_2V5
- GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only



GPU (M11) I/O Power

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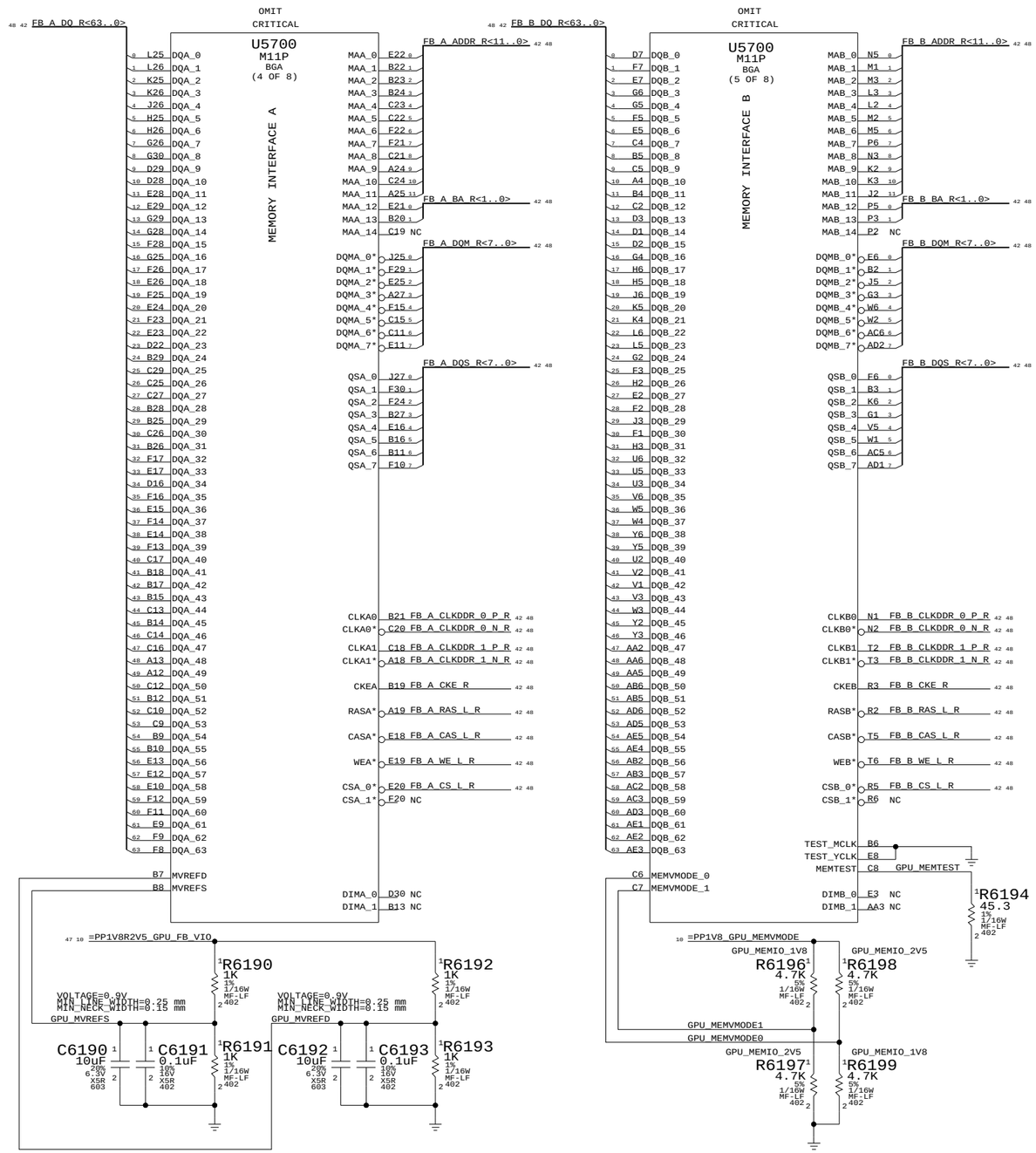
Page Notes

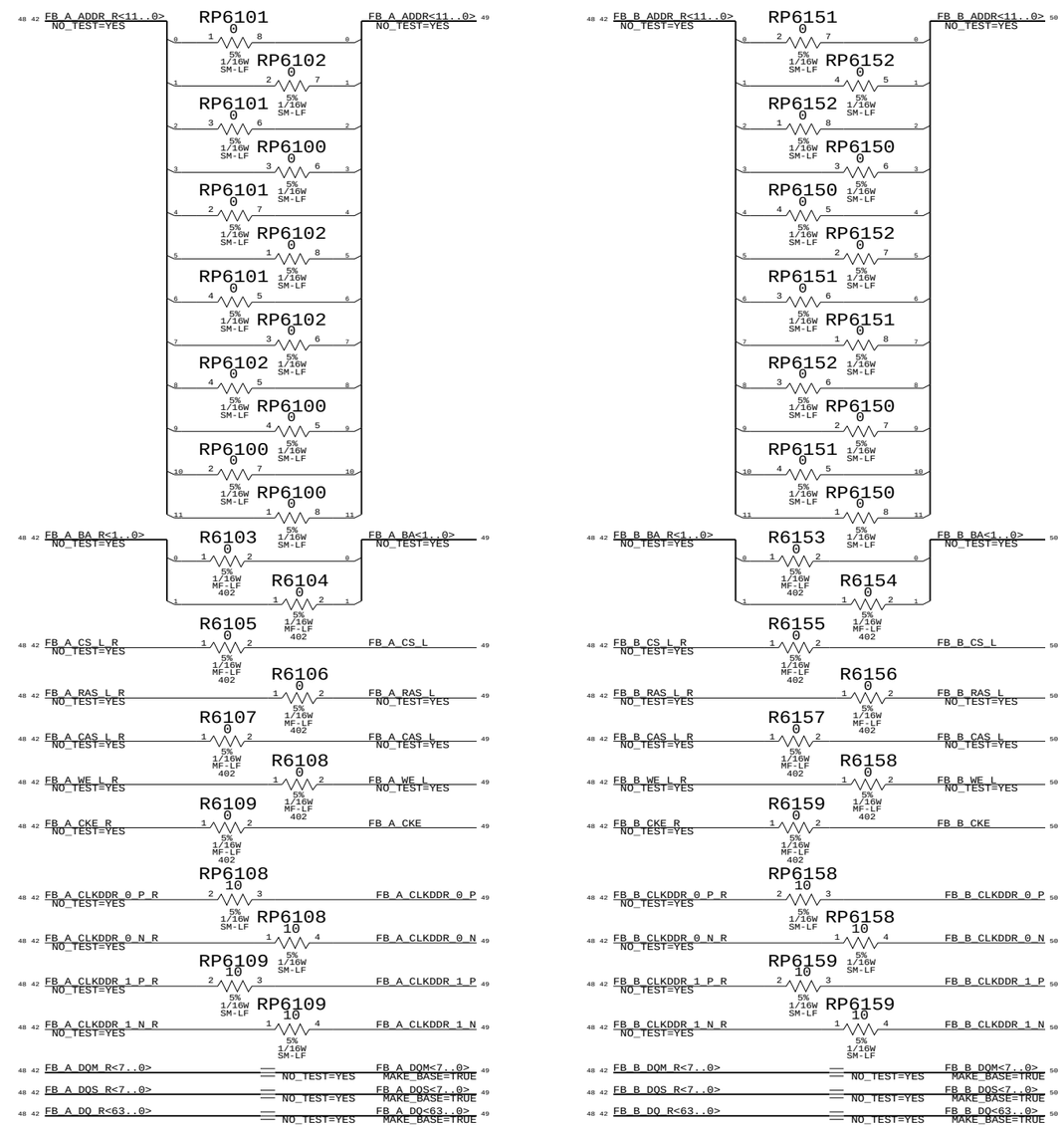
Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_MEMIO_1V8
- GPU_MEMIO_2V5



GPU Frame Buffer Series Term



GPU (M11) Frame Buffer I/F

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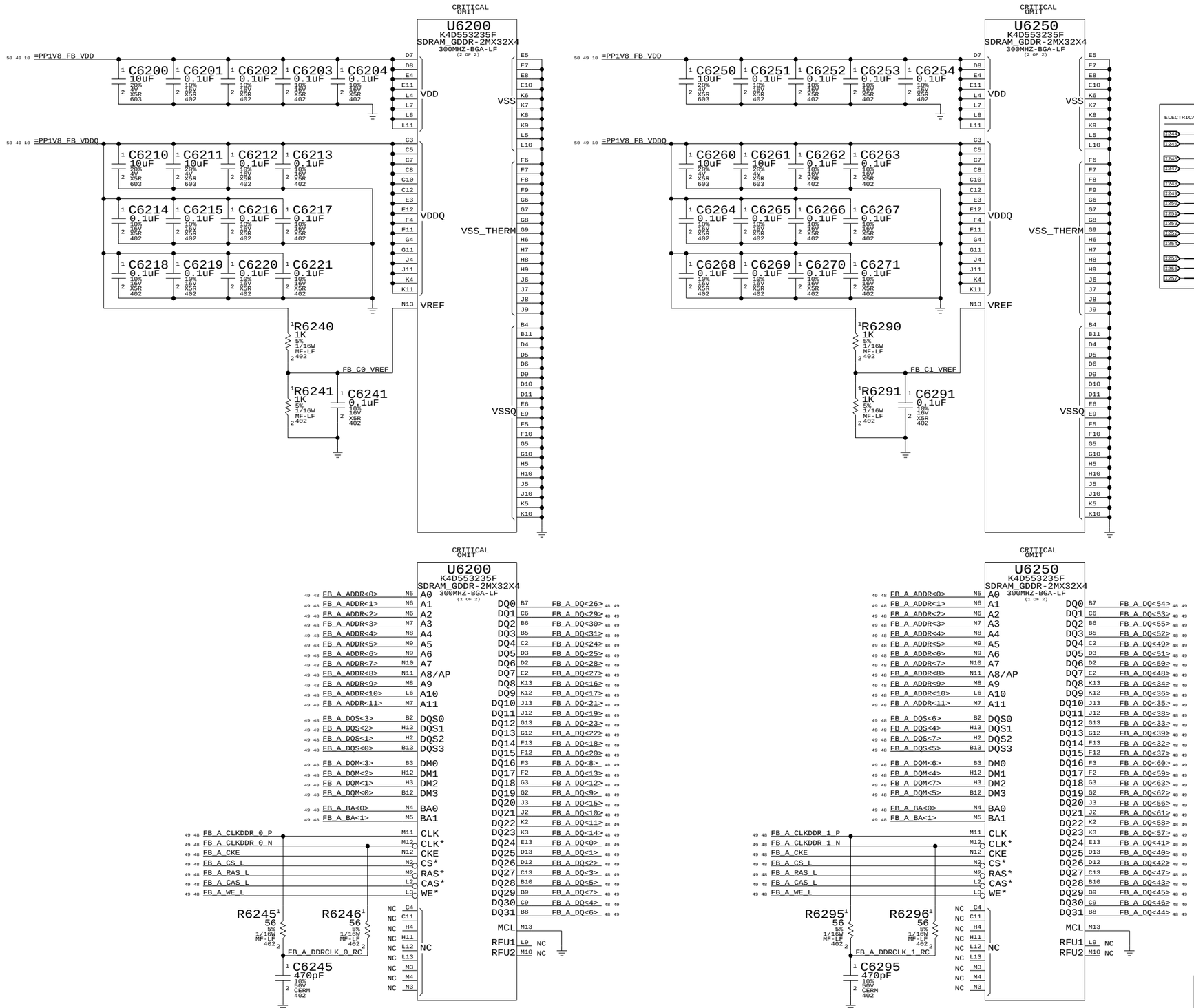

Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
E244	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_P
E245	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_N
E246	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_P
E247	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_N
E248	RAM	RAM		FB_A_CKE
E249	RAM	RAM		FB_A_CS_L
E250	RAM	RAM		FB_A_ADDR<11..0>
E251	RAM	RAM		FB_A_BA<1..0>
E253	RAM	RAM		FB_A_RAS_L
E252	RAM	RAM		FB_A_CAS_L
E254	RAM	RAM		FB_A_WE_L
E255	RAM	RAM		FB_A_DQS<7..0>
E256	RAM	RAM		FB_A_DQM<7..0>
E257	RAM	RAM		FB_A_DQ<63..0>

ECSETs provided by GPU

GPU Frame Buffer A

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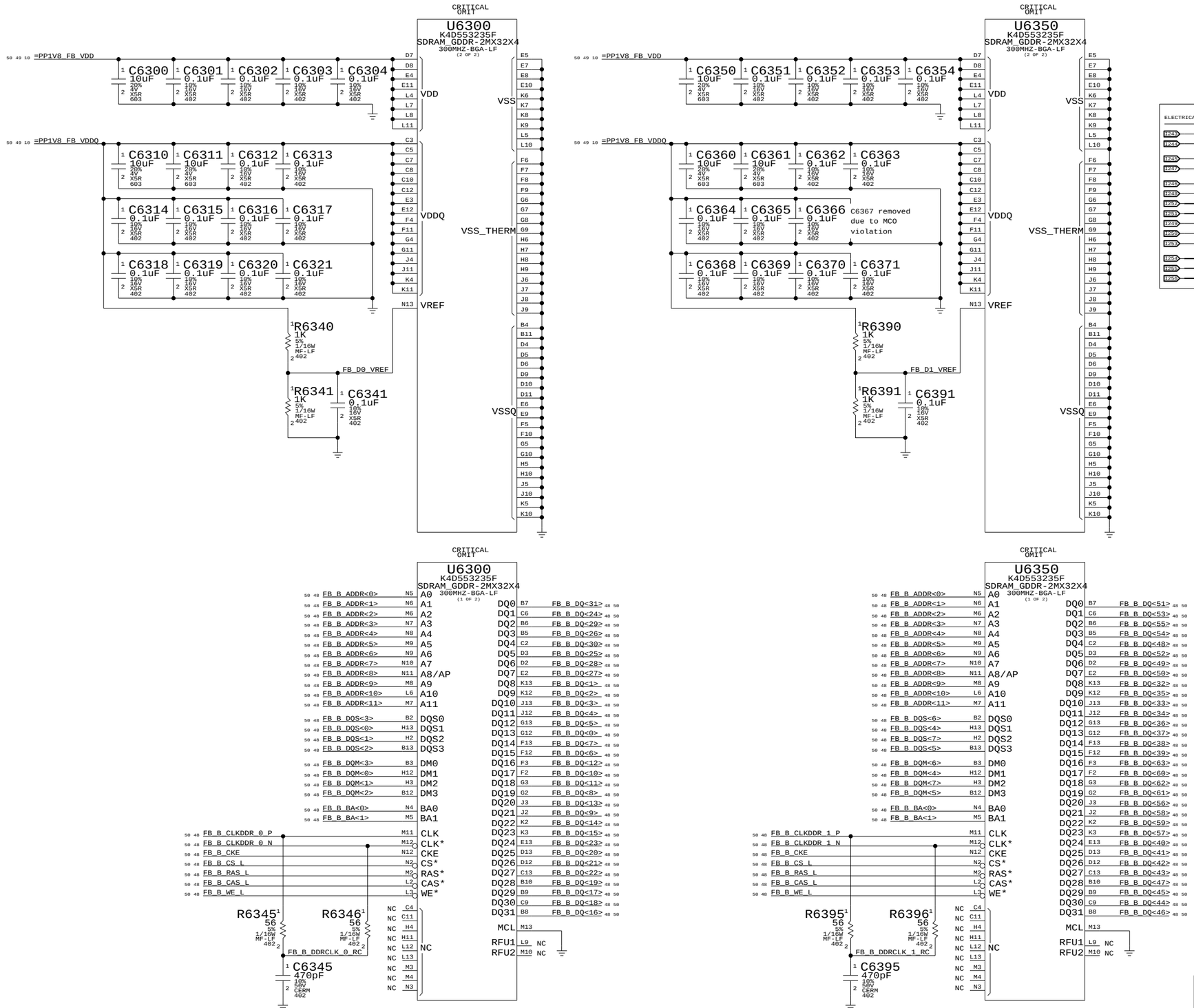

Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
I243	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_P
I244	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_N
I245	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_P
I247	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_N
I246	RAM	RAM		FB_B_CKE
I248	RAM	RAM		FB_B_CS_L
I282	RAM	RAM		FB_B_ADDR<11..0>
I251	RAM	RAM		FB_B_BA<1..0>
I249	RAM	RAM		FB_B_RAS_L
I250	RAM	RAM		FB_B_CAS_L
I253	RAM	RAM		FB_B_WE_L
I254	RAM	RAM		FB_B_DQS<7..0>
I255	RAM	RAM		FB_B_DQM<7..0>
I256	RAM	RAM		FB_B_DQ<63..0>

EE SETs provided by GPU

GPU Frame Buffer B

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SIZE	DRAWING NUMBER	REV.
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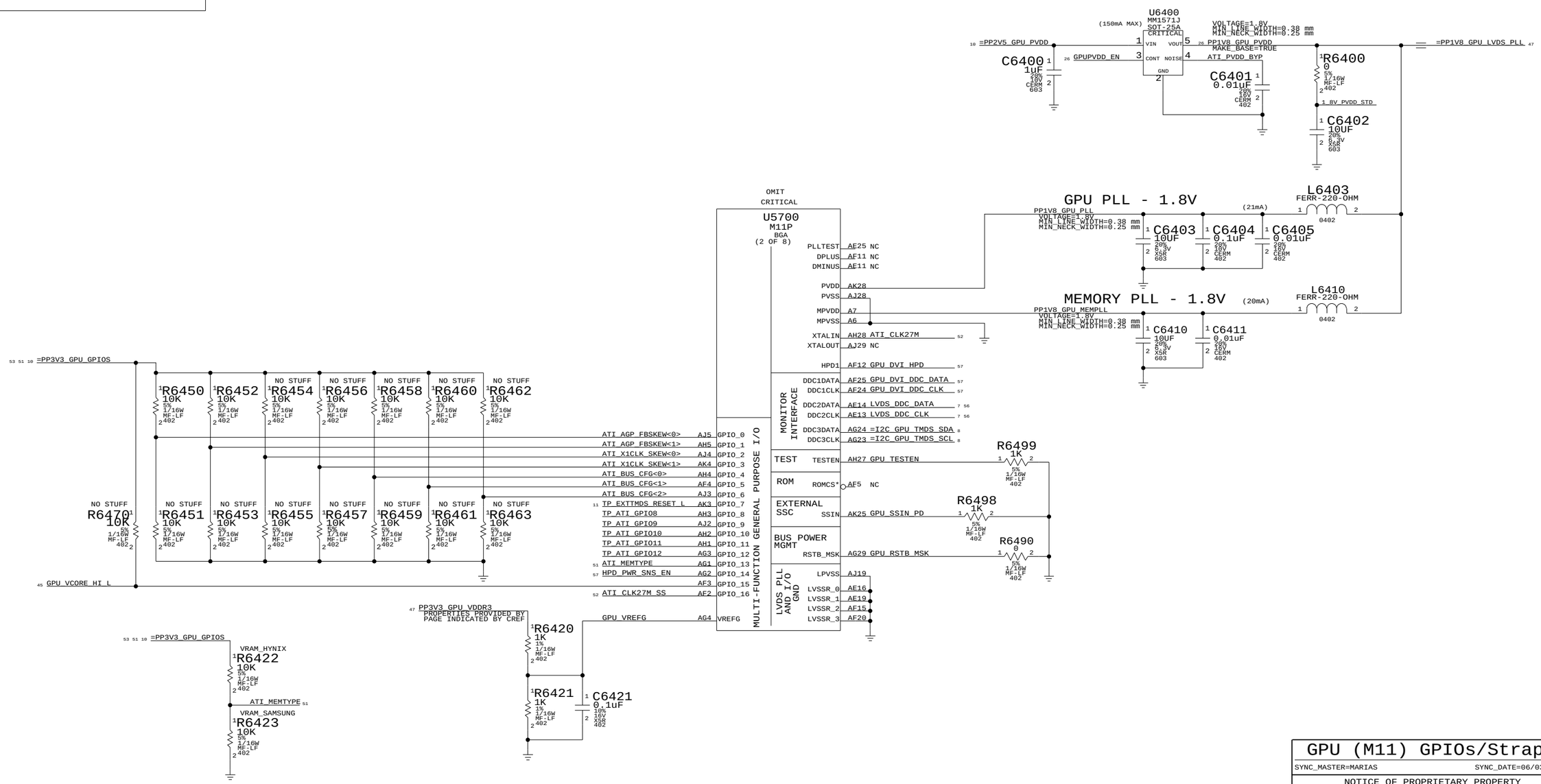
Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



GPU (M11) GPIOs/Straps

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SIZE	DRAWING NUMBER	REV.
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Page Notes

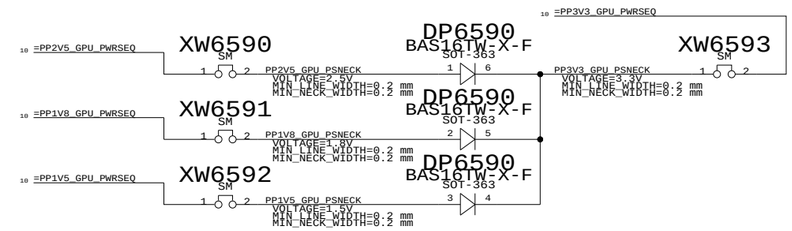
Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

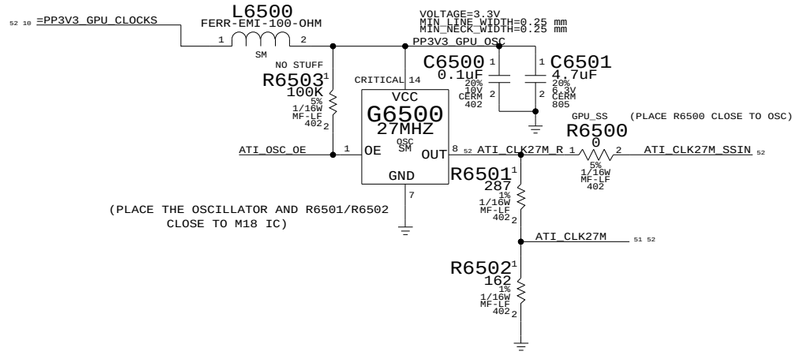
BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
163 ATI_CLK27M	CLOCK	CLOCK		ATI_CLK27M_R 52
164	CLOCK	CLOCK		ATI_CLK27M 51 52
165	CLOCK	CLOCK		ATI_CLK27M_SSIN 52
161 ATI_CLK27M_SS	CLOCK	CLOCK		ATI_CLK27M_SS_R 52
162	CLOCK	CLOCK		ATI_CLK27M_SS 51 52

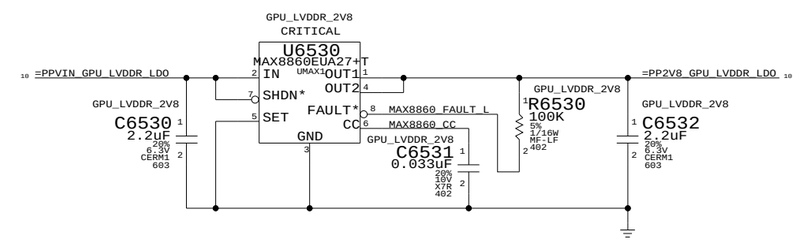
M11 Power Shutdown Sequencing



27M OSC



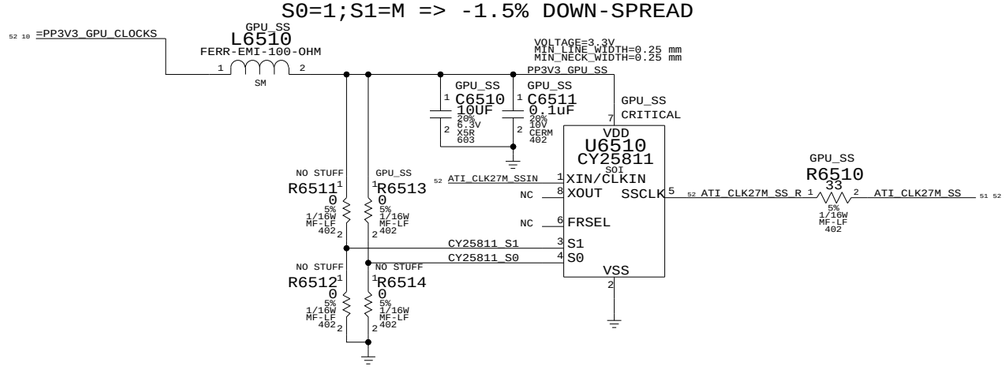
LVDDR 2.8V LDO



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S1140	GPU_LVDDR_2V8	U6530	2.82V instead of 2.77V

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD



GPU (M11) Clocks/Misc

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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D	051-6839	02

SCALE NONE SHT 65 OF 115

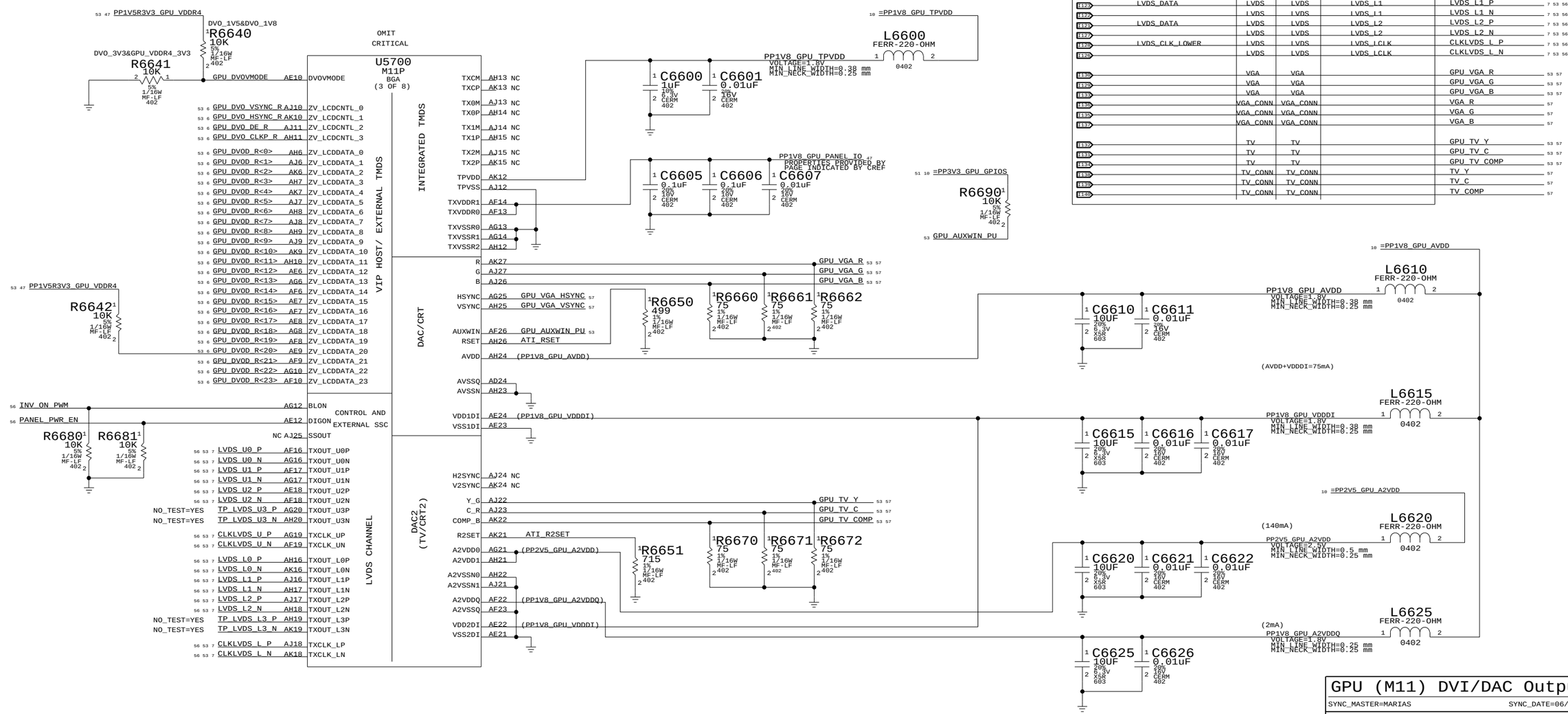
Page Notes

Power aliases required by this page:
- =PP2V5_GPU_A2VDD
- =PP1V8_GPU_AVDD
- =PP1V8_GPU_TPVDD
- =PP3V3_GPU_GPIOS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- GPU_VDDR4_3V3
- DVO_1V8
- DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
I100	DVO	DVO		GPU_DVOD_R<23..0>	6 53
I109 ECSETs provided by SI TMDS	DVO	DVO		GPU_DVO_HSYNC_R	6 53
I111	DVO	DVO		GPU_DVO_VSYNC_R	6 53
I110	DVO	DVO		GPU_DVO_DE_R	6 53
I112	DVO	DVO		GPU_DVO_CLKP_R	6 53
I113 LVDS_DATA	LVDS	LVDS	LVDS_U0	LVDS_U0_P	7 53 56
I114	LVDS	LVDS	LVDS_U0	LVDS_U0_N	7 53 56
I115 LVDS_DATA	LVDS	LVDS	LVDS_U1	LVDS_U1_P	7 53 56
I116	LVDS	LVDS	LVDS_U1	LVDS_U1_N	7 53 56
I117 LVDS_DATA	LVDS	LVDS	LVDS_U2	LVDS_U2_P	7 53 56
I118	LVDS	LVDS	LVDS_U2	LVDS_U2_N	7 53 56
I119 LVDS_CLK_UPPER	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_P	7 53 56
I120	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_N	7 53 56
I121 LVDS_DATA	LVDS	LVDS	LVDS_L0	LVDS_L0_P	7 53 56
I122	LVDS	LVDS	LVDS_L0	LVDS_L0_N	7 53 56
I123 LVDS_DATA	LVDS	LVDS	LVDS_L1	LVDS_L1_P	7 53 56
I124	LVDS	LVDS	LVDS_L1	LVDS_L1_N	7 53 56
I125 LVDS_DATA	LVDS	LVDS	LVDS_L2	LVDS_L2_P	7 53 56
I126	LVDS	LVDS	LVDS_L2	LVDS_L2_N	7 53 56
I127 LVDS_CLK_LOWER	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_P	7 53 56
I128	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_N	7 53 56
I129	VGA	VGA		GPU_VGA_R	53 57
I130	VGA	VGA		GPU_VGA_G	53 57
I131	VGA	VGA		GPU_VGA_B	53 57
I132	VGA_CONN	VGA_CONN		VGA_R	57
I133	VGA_CONN	VGA_CONN		VGA_G	57
I134	VGA_CONN	VGA_CONN		VGA_B	57
I135	TV	TV		GPU_TV_Y	53 57
I136	TV	TV		GPU_TV_C	53 57
I137	TV	TV		GPU_TV_COMP	53 57
I138	TV_CONN	TV_CONN		TV_Y	57
I139	TV_CONN	TV_CONN		TV_C	57
I140	TV_CONN	TV_CONN		TV_COMP	57



GPU (M11) DVI/DAC Outputs

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 66 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
- =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
- =SI_I2C_CLK
- =SI_I2C_DATA

BOM options provided by this page:
- TMDS_EXT - DVO_1V5 - DVO_3V3
- TMDS_DUAL - DVO_1V8

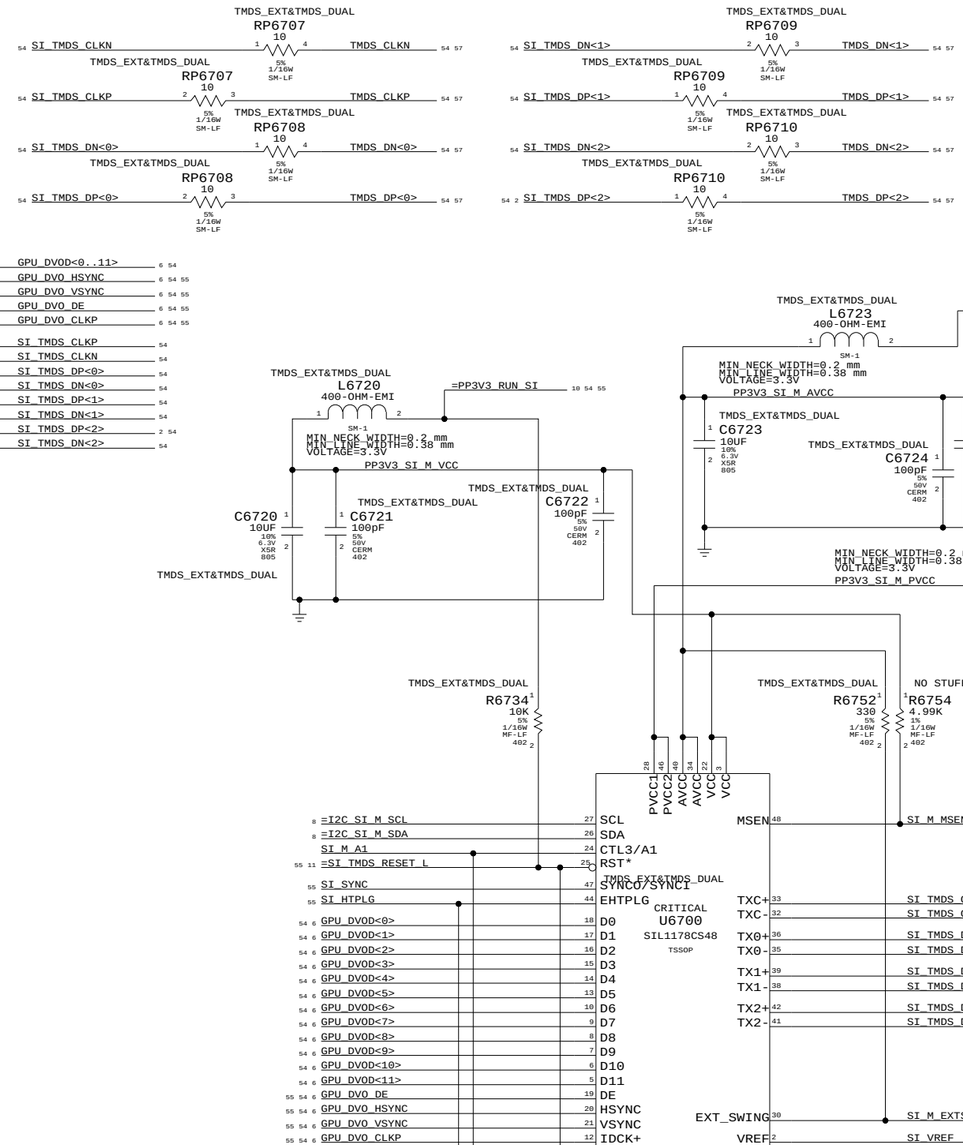
Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
GPU_DVO_LOWER	DVO	DVO		GPU_DVOD<0..11>	6 54
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_HSYNC	6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_VSYNC	6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_DE	6 54 55
GPU_DVO_CLKP	DVO	DVO		GPU_DVO_CLKP	6 54 55
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP	54
	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DP<0>	54
	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DN<0>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DP<1>	54
	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DN<1>	54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DP<2>	2 54
	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DN<2>	54

SILICON IMAGE TMDS

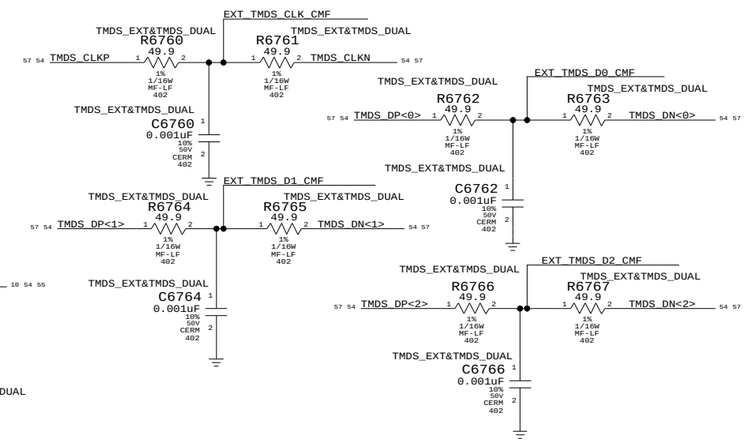


The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
	TMDS	TMDS	TMDS_CLK	TMDS_CLKP	54 57
	TMDS	TMDS	TMDS_CLK	TMDS_CLKN	54 57
	TMDS	TMDS	TMDS_D0	TMDS_DP<0>	54 57
	TMDS	TMDS	TMDS_D0	TMDS_DN<0>	54 57
	TMDS	TMDS	TMDS_D1	TMDS_DP<1>	54 57
	TMDS	TMDS	TMDS_D1	TMDS_DN<1>	54 57
	TMDS	TMDS	TMDS_D2	TMDS_DP<2>	54 57
	TMDS	TMDS	TMDS_D2	TMDS_DN<2>	54 57

EXTERNAL TMDS TERMINATION

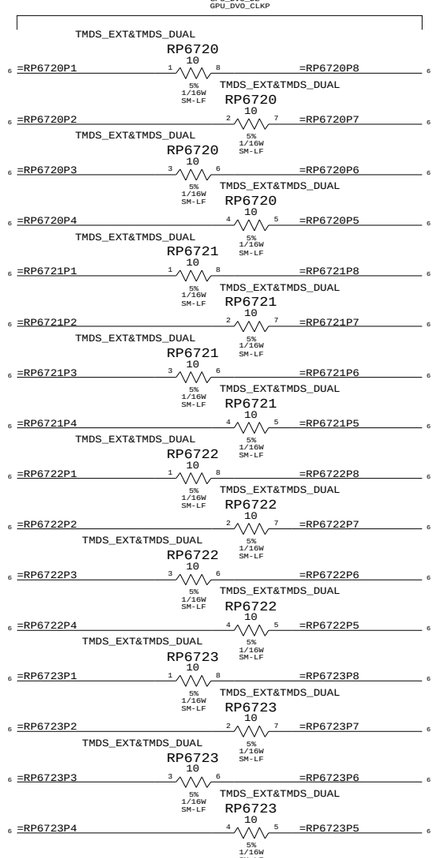
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN



Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>
GPU_DVO_HSYNC
GPU_DVO_VSYNC
GPU_DVO_DE
GPU_DVO_CLKP



Lower TMDS Transmitter

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 67 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI

Signal aliases required by this page:
- =SI_I2C_CLK
- =SI_I2C_DATA
- =SI_TMDS_RESET_L
- =RP68xxPy (pinswappable series R)

BOM options provided by this page:
- TMDS_DUAL

Net Spacing Type: TMDS

Net Physical Type: TMDS

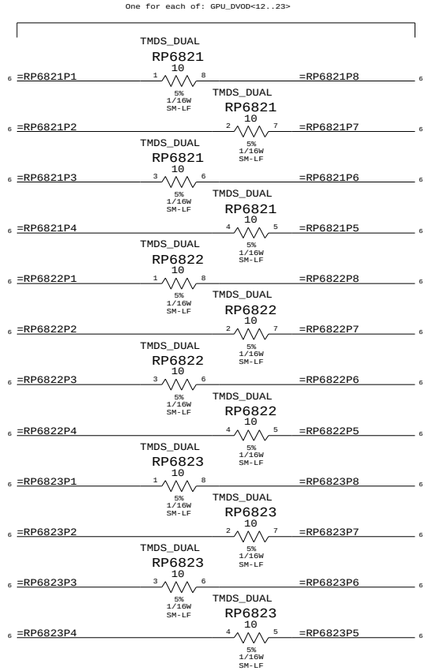
NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

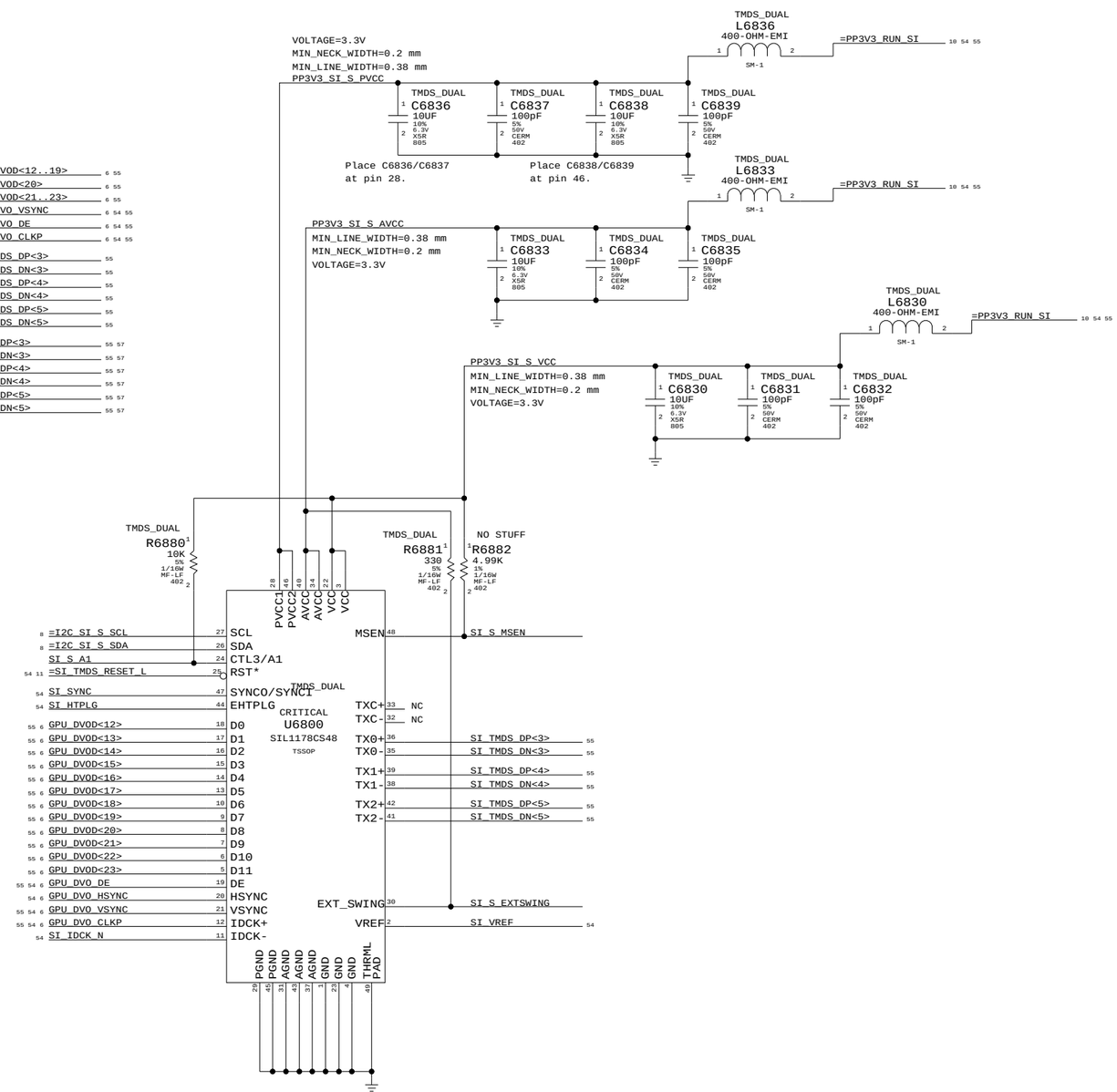
	ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
154	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<12..19>	6 55
155	GPU_DVOD20	DVO	DVO		GPU_DVOD<20>	6 55
156	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<21..23>	6 55
157		PROVIDED BY LOWER TXMR			GPU_DVO_VSYNC	6 54 55
158		PROVIDED BY LOWER TXMR			GPU_DVO_DE	6 54 55
159		PROVIDED BY LOWER TXMR			GPU_DVO_CLKP	6 54 55
160						
174	TMDS_DATA	TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DP<3>	55
175		TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DN<3>	55
176	TMDS_DATA	TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DP<4>	55
177		TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DN<4>	55
178	TMDS_DATA	TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DP<5>	55
179		TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DN<5>	55
180		TMDS	TMDS	TMDS_D3	TMDS_DP<3>	55 57
181		TMDS	TMDS	TMDS_D3	TMDS_DN<3>	55 57
182		TMDS	TMDS	TMDS_D4	TMDS_DP<4>	55 57
183		TMDS	TMDS	TMDS_D4	TMDS_DN<4>	55 57
184		TMDS	TMDS	TMDS_D5	TMDS_DP<5>	55 57
185		TMDS	TMDS	TMDS_D5	TMDS_DN<5>	55 57

Upper DVO series termination

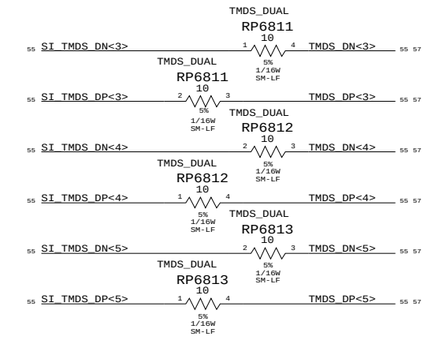
Place close to GPU

One for each of: GPU_DVOD<12..23>

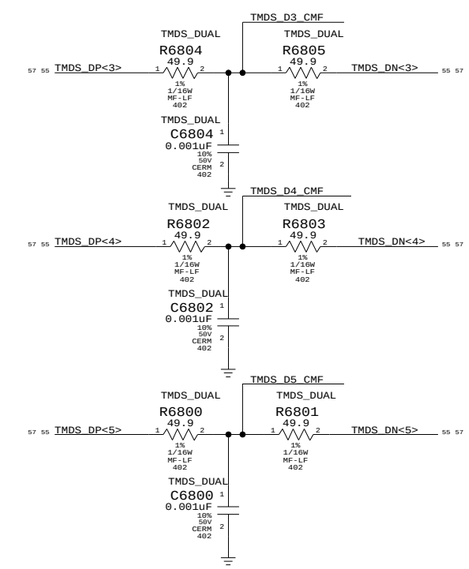




Upper Channel Series Termination



Upper Channel Common-mode Termination



Upper TMDS Transmitter

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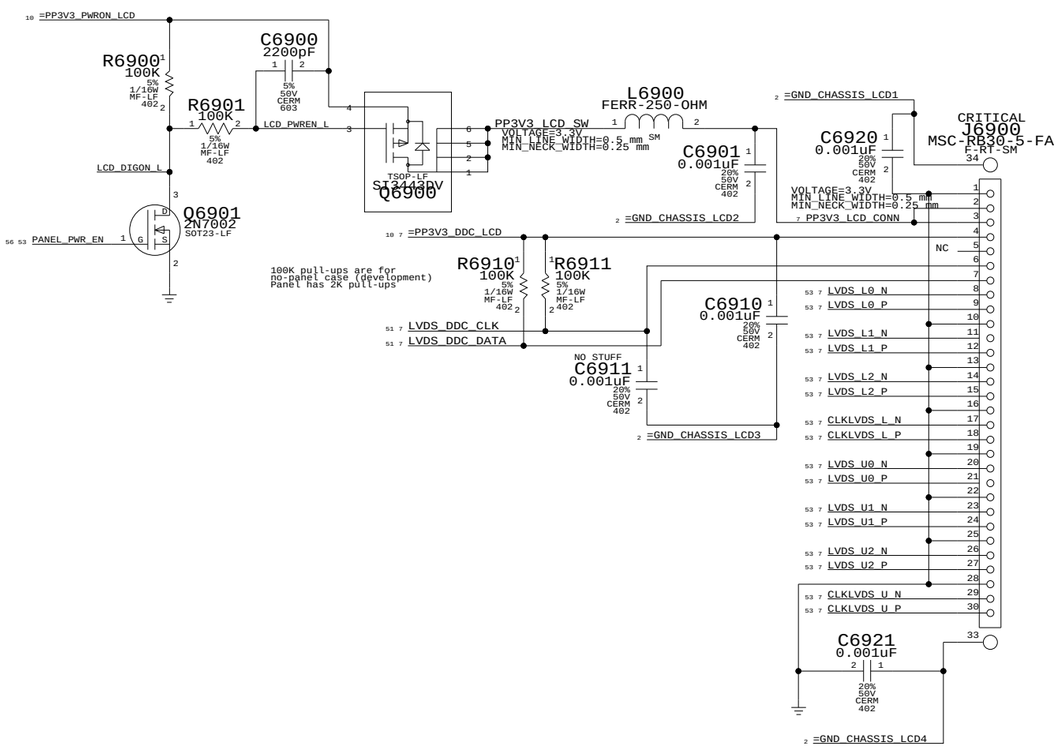
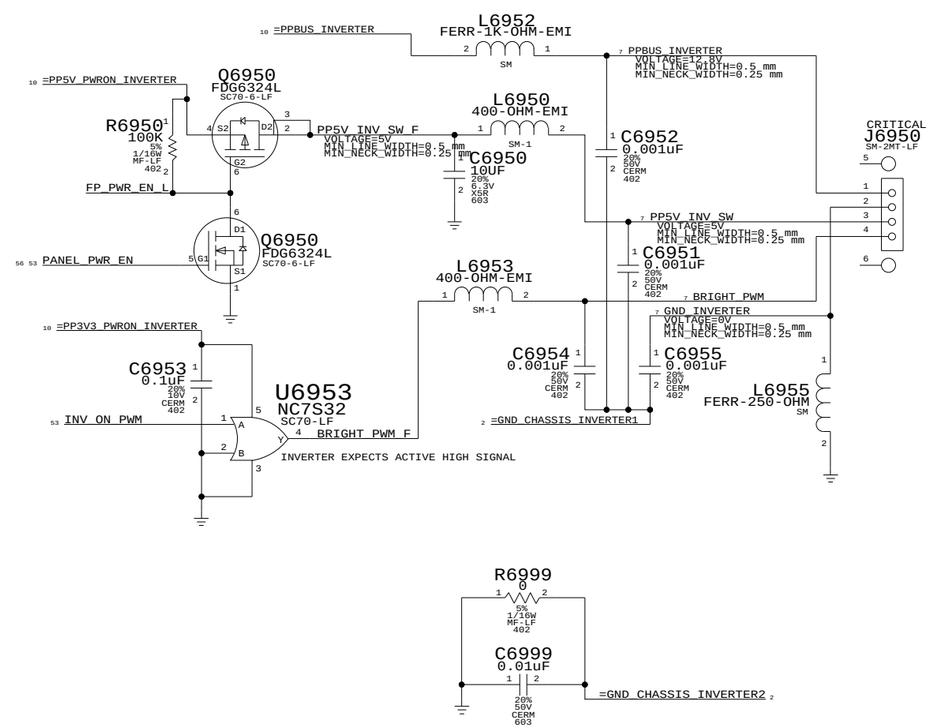
LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

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DVI INTERFACE

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
1540	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKP
1540	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKN
1590	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DP<0>
1591	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DN<0>
1592	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DP<1>
1593	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DN<1>
1594	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DP<2>
1595	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DN<2>
1596	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DP<3>
1597	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DN<3>
1598	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DP<4>
1599	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DN<4>
1600	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DP<5>
1601	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DN<5>

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

CRITICAL L7000 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<0> 1 — 4 TMDS_CONN_DN<0> 57
54 TMDS_DP<0> 2 — 3 TMDS_CONN_DP<0> 57

CRITICAL L7001 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<1> 1 — 4 TMDS_CONN_DN<1> 57
54 TMDS_DP<1> 2 — 3 TMDS_CONN_DP<1> 57

CRITICAL L7002 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<2> 1 — 4 TMDS_CONN_DN<2> 57
54 TMDS_DP<2> 2 — 3 TMDS_CONN_DP<2> 57

CRITICAL L7006 370-OHM SM SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_CLKP 1 — 4 TMDS_CONN_CLKP 57
54 TMDS_CLKN 2 — 3 TMDS_CONN_CLKN 57

CRITICAL L7003 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<3> 1 — 4 TMDS_CONN_DN<3> 57
55 TMDS_DP<3> 2 — 3 TMDS_CONN_DP<3> 57

CRITICAL L7004 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<4> 1 — 4 TMDS_CONN_DN<4> 57
55 TMDS_DP<4> 2 — 3 TMDS_CONN_DP<4> 57

CRITICAL L7005 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<5> 1 — 4 TMDS_CONN_DN<5> 57
55 TMDS_DP<5> 2 — 3 TMDS_CONN_DP<5> 57

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

10 =PP5V_RUN_DVI_DDC — CRITICAL F7010 0.5AMP-13.2V SM-LF — PP5V_RUN_DDC_FUSE VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

L7010 400-OHM-EMI SM-1 — PP5V_RUN_DDC 57 VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

Isolation required for DVI power switch

CRITICAL J7000 QH81127-CK1 F-RT-TH-LF

57 TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2> 57
		9	TMDS_CONN_DN<1> 57
57 TMDS_CONN_DP<0>	18	2	TMDS_CONN_DP<2> 57
		10	TMDS_CONN_DP<1> 57
	19	3	
57 TMDS_CONN_DN<5>	20	4	TMDS_CONN_DN<4> 57
		12	TMDS_CONN_DN<3> 57
57 TMDS_CONN_DP<5>	21	5	TMDS_CONN_DP<4> 57
		13	TMDS_CONN_DP<3> 57
	22	6	57 DVI_DDC_CLK_UF
		14	(PP5V_RUN_DDC)
57 TMDS_CONN_CLKP	23	7	DVI_DDC_DATA_UF
		15	
57 TMDS_CONN_CLKN	24	8	VGA_VSYNC 57
		16	57 DVI_HPD_UF
57 53 VGA_B	C3	C1	VGA_R 53 57
	C5B	C5A	
57 VGA_HSYNC	C4	C2	VGA_G 53 57
	34	32	
		35	

=GND_CHASSIS_DVI1 2
=GND_CHASSIS_DVI2 2

C7010 0.01uF 20% 50V CERM 603 — PLACE NEAR C5A & C5B

R7030 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI3 2

R7031 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI4 2

PLACE NEAR 3, 11 & 19

3V LEVEL SHIFTERS

D7010 SOD-123 — B0530WXF

PP5V_RUN_DDC_PULLUPS VOLTAGE=5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

R7010[1] 4.7K 5% 1/16W MF-LF 402

R7012[1] 4.7K 5% 1/16W MF-LF 402

C7011 100pF 5% 50V CERM 402

C7013 100pF 5% 50V CERM 402

C7014 100pF 5% 50V CERM 402

57 10 =PP3V3_DDC_DVI

Q7011 2N7002DW-X-F SOT-363	R7011 100 5% 1/16W MF-LF 402	DVI_DDC_CLK	R7020[1] 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_CLK 51
Q7011 2N7002DW-X-F SOT-363	R7013 100 5% 1/16W MF-LF 402	DVI_DDC_DATA	R7021[1] 10K 5% 1/16W MF-LF 402 — GPU_DVI_DDC_DATA 51
Q7014 2N7002DW-X-F SOT-363	R7014 100 5% 1/16W MF-LF 402	DVI_HPD	R7022[1] 100K 5% 1/16W MF-LF 402 — GPU_DVI_HPD 51

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

VGA SYNC BUFFERS

C7050 0.1uF 20% 10V CERM 402

57 10 =PP3V3_PWRON_VGASYNC — U7050 74AHC1G32 SM-LF — 53 GPU_VGA_VSYNC — GPU_VGA_VSYNC_BUF — R7050 33 5% 1/16W MF-LF 402 — VGA_VSYNC 57

PLACE R7050 & R7051 CLOSE TO DVI CONNECTOR

C7051 0.1uF 20% 10V CERM 402

57 10 =PP3V3_PWRON_VGASYNC — U7051 74AHC1G32 SM-LF — 53 GPU_VGA_HSYNC — GPU_HSYNC_BUF — R7051 33 5% 1/16W MF-LF 402 — VGA_HSYNC 57

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

FL7040 LCFILTER SM-220MHZ-LF CRITICAL — 53 GPU_VGA_B — VGA_B 53 57
C7040 3.3pF 0.25% 50V CERM 402 — R7040[1] 75 1% 1/16W MF-LF 402 NO STUFF

FL7041 LCFILTER SM-220MHZ-LF CRITICAL — 53 GPU_VGA_G — VGA_G 53 57
C7041 3.3pF 0.25% 50V CERM 402 — R7041[1] 75 1% 1/16W MF-LF 402 NO STUFF

FL7042 LCFILTER SM-220MHZ-LF CRITICAL — 53 GPU_VGA_R — VGA_R 53 57
C7042 3.3pF 0.25% 50V CERM 402 — R7042[1] 75 1% 1/16W MF-LF 402 NO STUFF

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW7060 SM — GND_GPU_TV1 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm — L7060 FERR-10-OHM-500MA SM — GND_TV1 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7060 0.01uF 20% 50V CERM 603

53 GPU_TV_Y	L7062 3.3uH 0603	53 TV_Y	C7062 560pF 10% 50V CERM 402 — C7063 560pF 10% 50V CERM 402
53 GPU_TV_C	L7064 3.3uH 0603	53 TV_C	C7064 560pF 10% 50V CERM 402 — C7065 560pF 10% 50V CERM 402
53 GPU_TV_COMP	L7066 3.3uH 0603	53 TV_COMP	C7066 560pF 10% 50V CERM 402 — C7067 560pF 10% 50V CERM 402

CRITICAL J7060 MINIDIN RT-TH-LF MH11773-MR8N-7F — 4 3 2 1 5 8 10 9 11

Q16C/514-0265/MH11773-MR8A-7F
Q41C/514-0256/MH11773-MR8N-7F

XW7061 SM — GND_GPU_TV2 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm — L7061 FERR-10-OHM-500MA SM — GND_TV2 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7061 0.01uF 20% 50V CERM 603

2 =GND_CHASSIS_TV

Place GND shorts at graphics controller

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from GPU during shutdown. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

57 PP5V_RUN_DDC — Q7081 TP0610 SOT23-3 — 57 DVI_DDC_CLK_UF — DVI_TURN_ON — R7081 680 5% 1/16W MF-LF 402 — DVI_TURN_ON_ILIM — R7083 10K 5% 1/16W MF-LF 402 — DVI_TURN_ON_BASE — Q7080 MMDT3904XF SOT-363-LF — SYS_POWER_BUTTON_L 24 25 30 36

R7082[1] 330 5% 1/16W MF-LF 402

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

57 10 =PP3V3_DDC_DVI — R7072[1] 68.1K 1% 1/16W MF-LF 402 — C7070 0.1uF 20% 10V CERM 402

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. Comparator output enabled by GPU.

HPD_4V_REF — U7070 LMC7211 SM-LF — HPD_PWR_SW — Q7076 2N7002DW-X-F SOT-363 — HPD_ON — R7078 330 5% 1/16W MF-LF 402 — HPD_ON_RC — R7080 20K 5% 1/16W MF-LF 402 — HPD_BASE — Q7080 MMDT3904XF SOT-363-LF

57 DVI_HPD_UF — R7070 10K 1% 1/16W MF-LF 402 — DVI_HPD_DIV — R7071[1] 10K 1% 1/16W MF-LF 402 — R7073[1] 100K 1% 1/16W MF-LF 402

10 =PPBUS_DVI_PWRSW — Q7075 TP0610 SOT23-3 — COMP_ENABLE — R7075[1] 100K 5% 1/16W MF-LF 402 — R7077[1] 100K 5% 1/16W MF-LF 402 — COMP_DISABLE

C7079 47uF 20% 6.3V CERM 1210 — R7079[1] 68K 5% 1/16W MF-LF 402

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY

51 HPD_PWR_SNS_EN — Q7076 2N7002DW-X-F SOT-363 — R7076[1] 100K 5% 1/16W MF-LF 402

External Display Conns

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 70 OF 115	

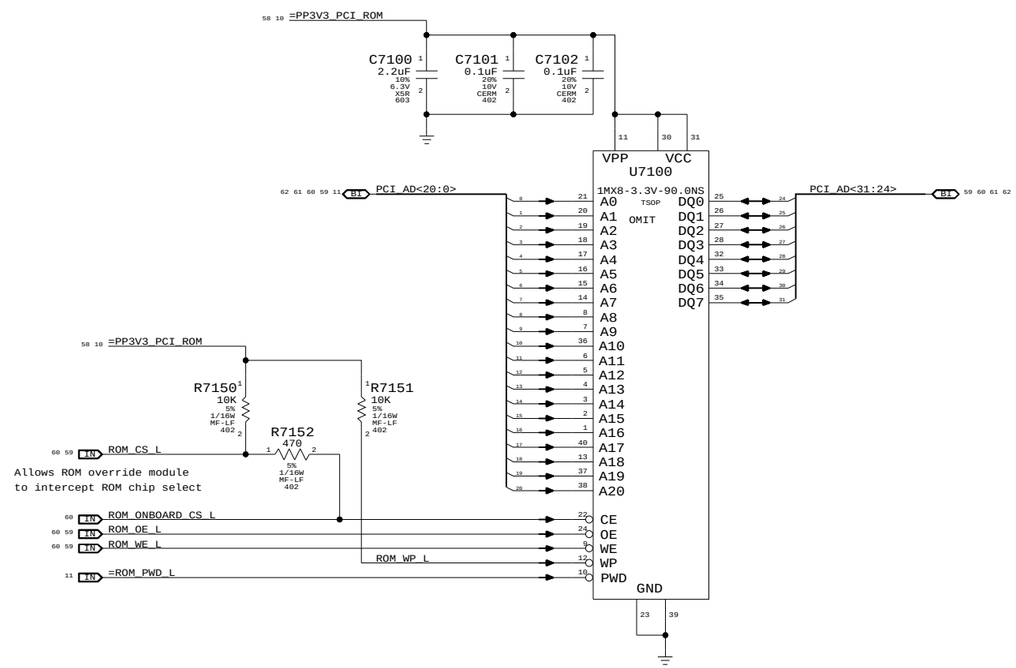
Page Notes

Power aliases required by this page:
- =PP3V3_PCI_ROM

Signal aliases required by this page:
- =ROM_PWD_L

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7100 part number.



BootROM

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 71 OF 115	

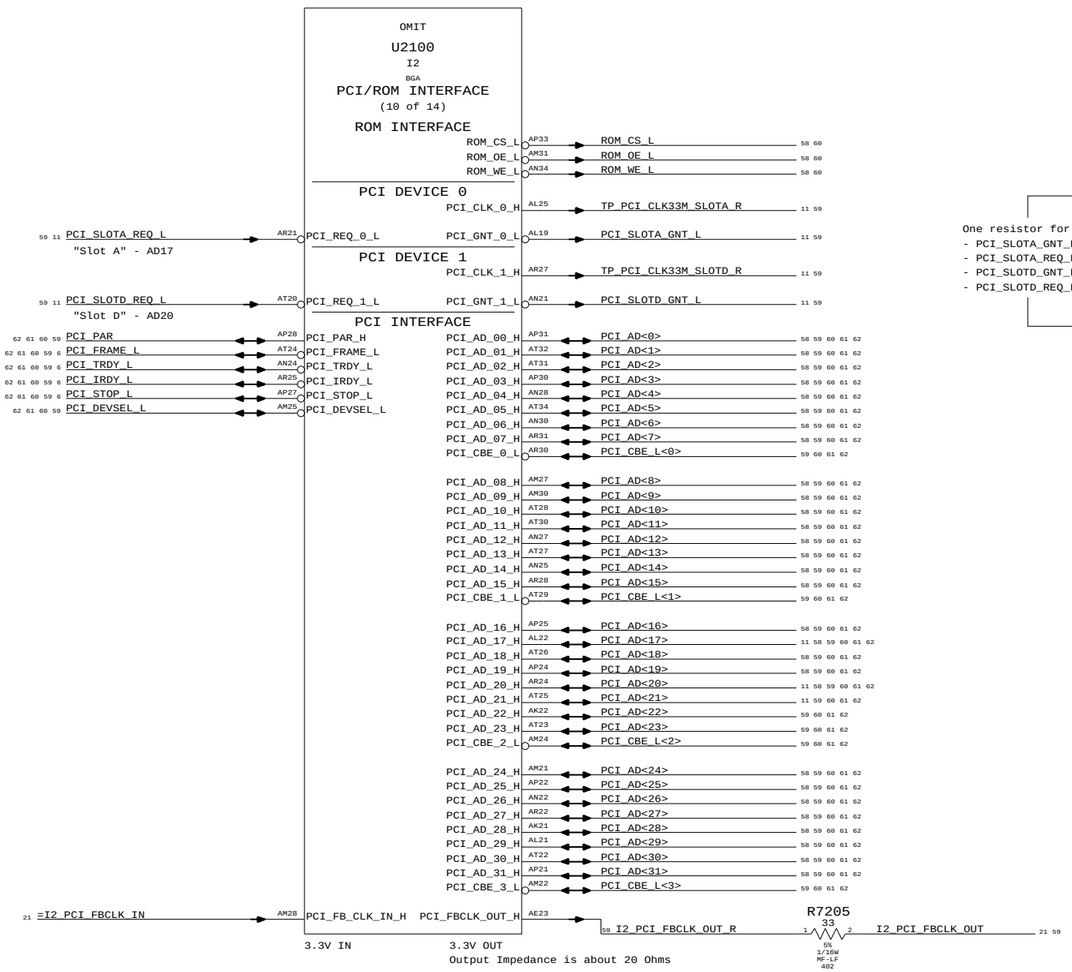
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
PCI_CLK_SLOTA	CLOCK	CLOCK		TP_PCI_CLK33M_SLOTA_R	11 59
PCI_CLK_SLOTD	CLOCK	CLOCK		TP_PCI_CLK33M_SLOTD_R	11 59
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_OUT_R	59
	I2_FBCLK	I2_FBCLK		I2_PCI_FBCLK_OUT	21 59
PCI_AD16_0	PCI	PCI		PCI_AD<16..0>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD17	PCI	PCI		PCI_AD<17>	11 58 59 60 61 62 (BOOTROM ADDR/SLOT A IDSEL)
PCI_AD19_18	PCI	PCI		PCI_AD<19..18>	58 59 60 61 62 (BOOTROM ADDR)
PCI_AD20	PCI	PCI		PCI_AD<20>	11 58 59 60 61 62 (SLOT D IDSEL)
PCI_AD21	PCI	PCI		PCI_AD<21>	11 59 60 61 62 (SLOT E IDSEL)
PCI_AD23_22	PCI	PCI		PCI_AD<23..22>	59 60 61 62 (PCI ONLY)
PCI_AD31_24	PCI	PCI		PCI_AD<31..24>	58 59 60 61 62 (BOOTROM DATA)
PCI_CBE	PCI	PCI		PCI_CBE_L<3..0>	59 60 61 62
PCI_CTL	PCI	PCI		PCI_FRAME_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_DEVSEL_L	59 60 61 62
PCI_CTL	PCI	PCI		PCI_IRDY_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_TRDY_L	6 59 60 61 62
PCI_CTL	PCI	PCI		PCI_STOP_L	6 59 60 61 62
PCI_PAR	PCI	PCI		PCI_PAR	59 60 61 62
	PCI	PCI		PCI_SLOTA_REQ_L	11 59
	PCI	PCI		PCI_SLOTA_GNT_L	11 59
	PCI	PCI		PCI_SLOTD_REQ_L	11 59
	PCI	PCI		PCI_SLOTD_GNT_L	11 59

Page Notes

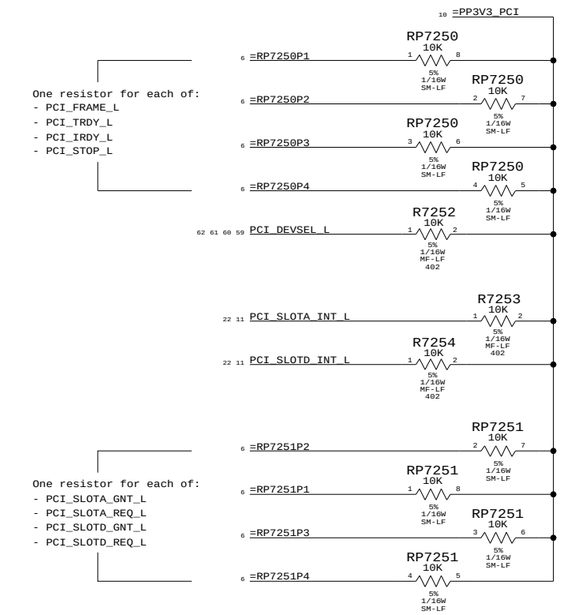
Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
- =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
(NONE)



PCI PULL-UPS



SLOT E REQ/GNT pull-ups
not provided by this page.

I2 PCI Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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D	051-6839	02
SCALE NONE	SHT 72 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

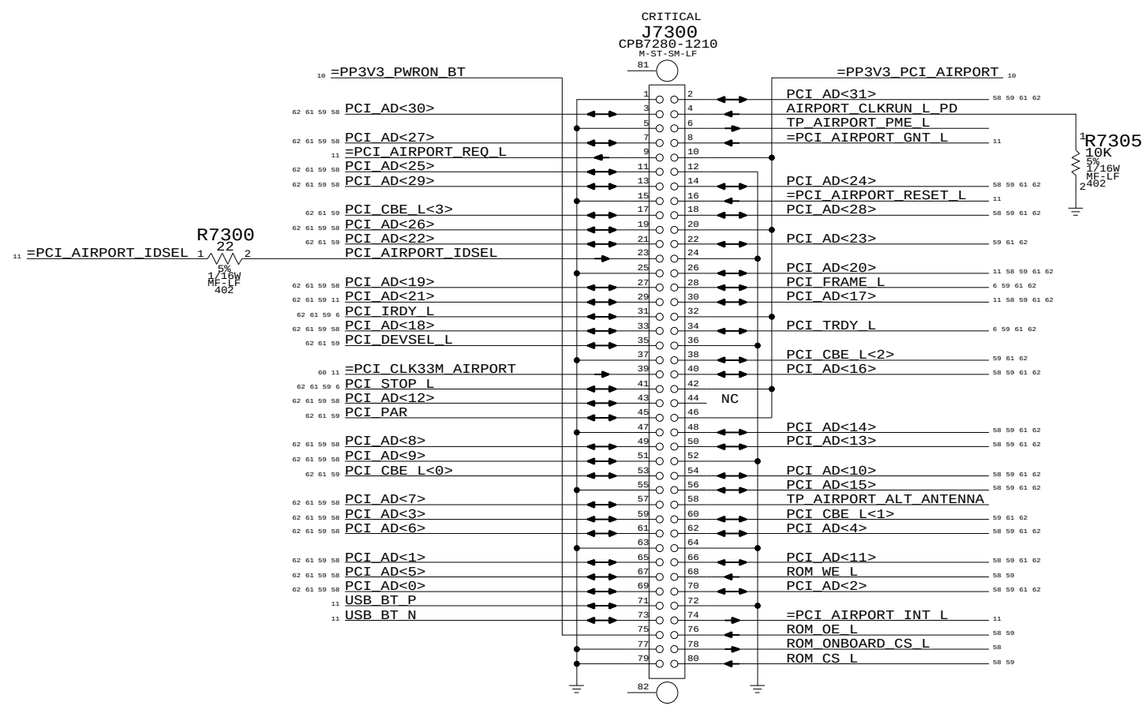
Power aliases required by this page:
- =PP3V3_PCI (802.11g Power)
- =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =USB_BT_P (Bluetooth USB D+)
- =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.



Q85 Connector
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

Q85 AIRPORT/BT CONN

SYNC_MASTER=MARIAS-MDIFF SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 73 OF 115	

NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI2	CLOCK	CLOCK	

=PCI_CLK33M_CBUS

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

=PP3V3_RUN_PCI1510_R — R7400 0 5% 1/10W MF-LF 603

PP3V3_RUN_PCI1510 VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C7400 10UF 20% 6.3V X5R 603 | C7401 10UF 20% 6.3V X5R 603 | C7402 0.22UF 10% 6.3V CERM-X5R 402 | C7403 0.22UF 10% 6.3V CERM-X5R 402 | C7404 0.22UF 10% 6.3V CERM-X5R 402

C7405 0.22UF 10% 6.3V CERM-X5R 402 | C7406 0.22UF 10% 6.3V CERM-X5R 402 | C7407 0.22UF 10% 6.3V CERM-X5R 402 | C7408 0.22UF 10% 6.3V CERM-X5R 402

R7410 10K 5% 1/10W MF-LF 402

=PP2V5_RUN_PCI1510 — C7410 4.7uF 20% 6.3V CERM 805 | C7411 0.22UF 10% 6.3V CERM-X5R 402

=PPS5V_PWRON_TPS2211
=PP3V3_PWRON_TPS2211
=TPS2211_SHDN_L — R7450 0 5% 1/10W MF-LF 402 — TPS2211_SHTDWN_L

U7450 TPS2211 SSOI

Pin	Signal
NC 9	V_12
5	V_5_1
6	V_5_2
3	V_3_1
4	V_3_2
1	VCCD0
2	VCCD1
15	VPPD0
14	VPPD1
16	SHTDWN
7	GND
10	AVPP
11	AVCC0
12	AVCC1
13	AVCC2
8 NC	OC

PPVPP_CBUS_SW VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm
PPVCC_CBUS_SW VOLTAGE=3.3V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C7450 0.1uF 20% 10V CERM 402 | C7451 0.1uF 20% 10V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

U7400 PCI1510ZGU BGA-LF

CRITICAL — CLAMP FOR PC-CARD/CCCB — CLAMP FOR PCI — VCCP

VCC: A7, C13, D5, E1, M1, N7, N11

Pin	Signal
NC H10	CLK_48_RSVD/NC
PCI1510_VR_EN_L D4	VR_EN*
L8	VR_PORT
B11	CCCB
L3	VCCP
N13	CBUS_VCCD0_L (VCCD0*)
L12	CBUS_VCCD1_L (VCCD1*)
K9	CBUS_VPPD0 (VPPD0)
M11	CBUS_VPPD1 (VPPD1)
L13	CBUS_DET_1_L (CD1*/CCD1*)
B5	CBUS_DET_2_L (CD2*/CCD2*)
F12	CBUS_IORD_L (IORD*/CAD13)
C11	CBUS_IOWR_L (IOWR*/CAD15)
G10	CBUS_OE_L (OE*/CAD11)
H13	CBUS_CE1_L (CE1*/CC/BE0*)
B2	CBUS_VS1 (VS1*/CVS1)
A9	CBUS_VS2 (VS2*/CVS2)
D13	CBUS_WE_L (WE*/CGNT*)
A6	CBUS_READY (RDY/IREQ*/CINT*)
D8	CBUS_RESET_L (RESET/CRST*)
A8	CBUS_REG_L (REG*/CC/BE3*)
C6	CBUS_BVD1_L (BVD1/CSTSCHG/STSCHG*/RI*)
D6	CBUS_BVD2_L (BVD2/SPKR*/CAUDIO)
A5	CBUS_WP_L (WP/IOIS16*/CCLKRUN*)
G13	CBUS_CE2_L (CE2/CAD10*)
B8	CBUS_INPACK_L (INPACK/CREQ*)
B6	CBUS_WAIT_L (WAIT/CSERR*)
C7	CBUS_ADDR<0> (A0/CAD26)
D7	CBUS_ADDR<1> (A1/CAD25)
B7	CBUS_ADDR<2> (A2/CAD24)
D10	CBUS_ADDR<3> (A3/CAD23)
B12	CBUS_ADDR<4> (A4/CAD22)
C8	CBUS_ADDR<5> (A5/CAD21)
C9	CBUS_ADDR<6> (A6/CAD20)
A12	CBUS_ADDR<7> (A7/CAD18)
E11	CBUS_ADDR<8> (A8/CC/BE1*)
F11	CBUS_ADDR<9> (A9/CAD14)
G11	CBUS_ADDR<10> (A10/CAD9)
G12	CBUS_ADDR<11> (A11/CAD12)
D9	CBUS_ADDR<12> (A12/CC/BE2*)
E12	CBUS_ADDR<13> (A13/CPAR)
D12	CBUS_ADDR<14> (A14/CPERR*)
C10	CBUS_ADDR<15> (A15/CIRDY*)
B13	CBUS_ADDR_16_R (A16/CCLK)
F10	CBUS_ADDR<17> (A17/CAD16)
E13	CBUS_ADDR<18> (A18/RSVD)
A13	CBUS_ADDR<19> (A19/CBLOCK*)
E10	CBUS_ADDR<20> (A20/CSTOP*)
D11	CBUS_ADDR<21> (A21/CDEVSEL*)
C12	CBUS_ADDR<22> (A22/CTRDY*)
A10	CBUS_ADDR<23> (A23/CFRAME*)
B10	CBUS_ADDR<24> (A24/CAD17)
B9	CBUS_ADDR<25> (A25/CAD19)
A4	CBUS_DATA<0> (D0/CAD27)
C4	CBUS_DATA<1> (D1/CAD29)
A3	CBUS_DATA<2> (D2/RSVD)
K11	CBUS_DATA<3> (D3/CAD0)
K12	CBUS_DATA<4> (D4/CAD1)
J13	CBUS_DATA<5> (D5/CAD3)
J10	CBUS_DATA<6> (D6/CAD5)
H12	CBUS_DATA<7> (D7/CAD7)
C5	CBUS_DATA<8> (D8/CAD28)
B4	CBUS_DATA<9> (D9/CAD30)
B3	CBUS_DATA<10> (D10/CAD31)
M12	CBUS_DATA<11> (D11/CAD2)
J11	CBUS_DATA<12> (D12/CAD4)
K13	CBUS_DATA<13> (D13/CAD6)
J12	CBUS_DATA<14> (D14/RSVD)
H11	CBUS_DATA<15> (D15/CAD8)
N8	PCI_AD<0> (AD0)
M7	PCI_AD<1> (AD1)
L7	PCI_AD<2> (AD2)
N6	PCI_AD<3> (AD3)
K4	PCI_AD<4> (AD4)
M6	PCI_AD<5> (AD5)
L6	PCI_AD<6> (AD6)
N5	PCI_AD<7> (AD7)
N4	PCI_AD<8> (AD8)
M2	PCI_AD<9> (AD9)
M5	PCI_AD<10> (AD10)
L4	PCI_AD<11> (AD11)
N3	PCI_AD<12> (AD12)
K5	PCI_AD<13> (AD13)
L5	PCI_AD<14> (AD14)
M4	PCI_AD<15> (AD15)
J4	PCI_AD<16> (AD16)
H1	PCI_AD<17> (AD17)
H3	PCI_AD<18> (AD18)
H2	PCI_AD<19> (AD19)
G2	PCI_AD<20> (AD20)
G4	PCI_AD<21> (AD21)
F1	PCI_AD<22> (AD22)
C3	PCI_AD<23> (AD23)
F3	PCI_AD<24> (AD24)
E2	PCI_AD<25> (AD25)
F4	PCI_AD<26> (AD26)
B1	PCI_AD<27> (AD27)
D2	PCI_AD<28> (AD28)
E4	PCI_AD<29> (AD29)
D3	PCI_AD<30> (AD30)
E3	PCI_AD<31> (AD31)
K6	PCI_CBE_L<0> (C/BE0*)
M3	PCI_CBE_L<1> (C/BE1*)
J2	PCI_CBE_L<2> (C/BE2*)
A1	PCI_CBE_L<3> (C/BE3*)
N1	PCI_PAR (PAR)
K1	PCI_IRDY_L (IRDY)
L2	PCI_SERR_L (SERR)
F2	PCI_CBUS_IDSEL (IDSEL)
K3	PCI_PERR_L (PERR)
J1	PCI_FRAME_L (FRAME)
L1	PCI_STOP_L (STOP)
J3	PCI_TRDY_L (TRDY)
K2	PCI_DEVSEL_L (DEVSEL)
B3	PCI_CBUS_RESET_L (PRST)
C2	=PCI_CBUS_REQ_L (REQ)
C1	=PCI_CBUS_GNT_L (GNT)
E1	=PCI_CLK33M_CBUS (PCLK)
M9	SPKROUT
M8	RI_OUT/PME
N10	CBUS_SUSPEND_PU (SUSPEND)
K7	=PCI_CBUS_INT_L (MFUNC0)
N9	CBUS_MFUNC1_PD (MFUNC1)
L9	CBUS_MFUNC2_PD (MFUNC2)
K10	CBUS_MFUNC3_PD (MFUNC3)
M10	CBUS_MFUNC4_PD (MFUNC4)
N12	CBUS_MFUNC5_PD (MFUNC5)
L10	CBUS_MFUNC6_PD (MFUNC6)
L11	GRST

INTEGRATED PULL-UP

GND: A2, A11, D1, F13, H4, K8, M13, N2

=PCI_CBUS_IDSEL — R7423 22 5% 1/10W MF-LF 402

=PCI_CBUS_RESET_L — R7424 47 5% 1/10W MF-LF 402

R7430 47 5% 1/16W MF-LF 402 — CBUS_ADDR<16>

PCI1510 PULL-UPS

PP3V3_RUN_PCI1510

R7420 10K 5% 1/10W MF-LF 402 — PCI_PERR_L
R7421 10K 5% 1/10W MF-LF 402 — PCI_SERR_L
R7422 10K 5% 1/10W MF-LF 402 — CBUS_SUSPEND_PU

RP7410 10K 5% 1/10W SM-LF
CBUS_MFUNC5_PD
CBUS_MFUNC6_PD
CBUS_MFUNC3_PD
CBUS_MFUNC1_PD

R7411 10K 5% 1/10W MF-LF 402 — CBUS_MFUNC4_PD

R7412 10K 5% 1/10W MF-LF 402 — CBUS_MFUNC2_PD

PC CARD/CARDBUS CONNECTOR

CRITICAL
J7490 QT500806-L121-9F M-ST-SM

Pin	Signal	Pin	Signal
2		1	CBUS_DATA<3>
4	CBUS_DET_1_L	3	CBUS_DATA<4>
6	CBUS_DATA<11>	5	CBUS_DATA<5>
8	CBUS_DATA<12>	7	CBUS_DATA<6>
10	CBUS_DATA<13>	9	
12		11	CBUS_DATA<7>
14	CBUS_DATA<14>	13	CBUS_CE1_L
16	CBUS_DATA<15>	15	CBUS_ADDR<10>
18	CBUS_CE2_L	17	CBUS_OE_L
20	CBUS_VS1	19	
22		21	CBUS_ADDR<11>
24	CBUS_IORD_L	23	CBUS_ADDR<9>
26	CBUS_IOWR_L	25	CBUS_ADDR<8>
28	CBUS_ADDR<17>	27	CBUS_ADDR<13>
30	CBUS_ADDR<18>	29	
32		31	CBUS_ADDR<14>
34	CBUS_ADDR<19>	33	CBUS_WE_L
36	CBUS_ADDR<20>	35	CBUS_READY
38	CBUS_ADDR<21>	37	PPVCC_CBUS_SW
40	PPVCC_CBUS_SW	39	
42		41	PPVPP_CBUS_SW
44	PPVPP_CBUS_SW	43	CBUS_ADDR<16>
46	CBUS_ADDR<22>	45	CBUS_ADDR<15>
48	CBUS_ADDR<23>	47	CBUS_ADDR<12>
50	CBUS_ADDR<24>	49	
52		51	CBUS_ADDR<7>
54	CBUS_ADDR<25>	53	CBUS_ADDR<6>
56	CBUS_VS2	55	CBUS_ADDR<5>
58	CBUS_RESET_L	57	CBUS_ADDR<4>
60	CBUS_WAIT_L	59	
62		61	CBUS_ADDR<3>
64	CBUS_INPACK_L	63	CBUS_ADDR<2>
66	CBUS_REG_L	65	CBUS_ADDR<1>
68	CBUS_BVD2_L	67	CBUS_ADDR<0>
70	CBUS_BVD1_L	69	
72		71	CBUS_DATA<0>
74	CBUS_DATA<8>	73	CBUS_DATA<1>
76	CBUS_DATA<9>	75	CBUS_DATA<2>
78	CBUS_DATA<10>	77	CBUS_WP_L
80	CBUS_DET_2_L	79	

B4, B1, B3, B2

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON PPVCC_CBUS_SW

C7490 2.2uF 10% 6.3V X5R 603 | C7491 2.2uF 10% 6.3V X5R 603

Cardbus

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 74 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

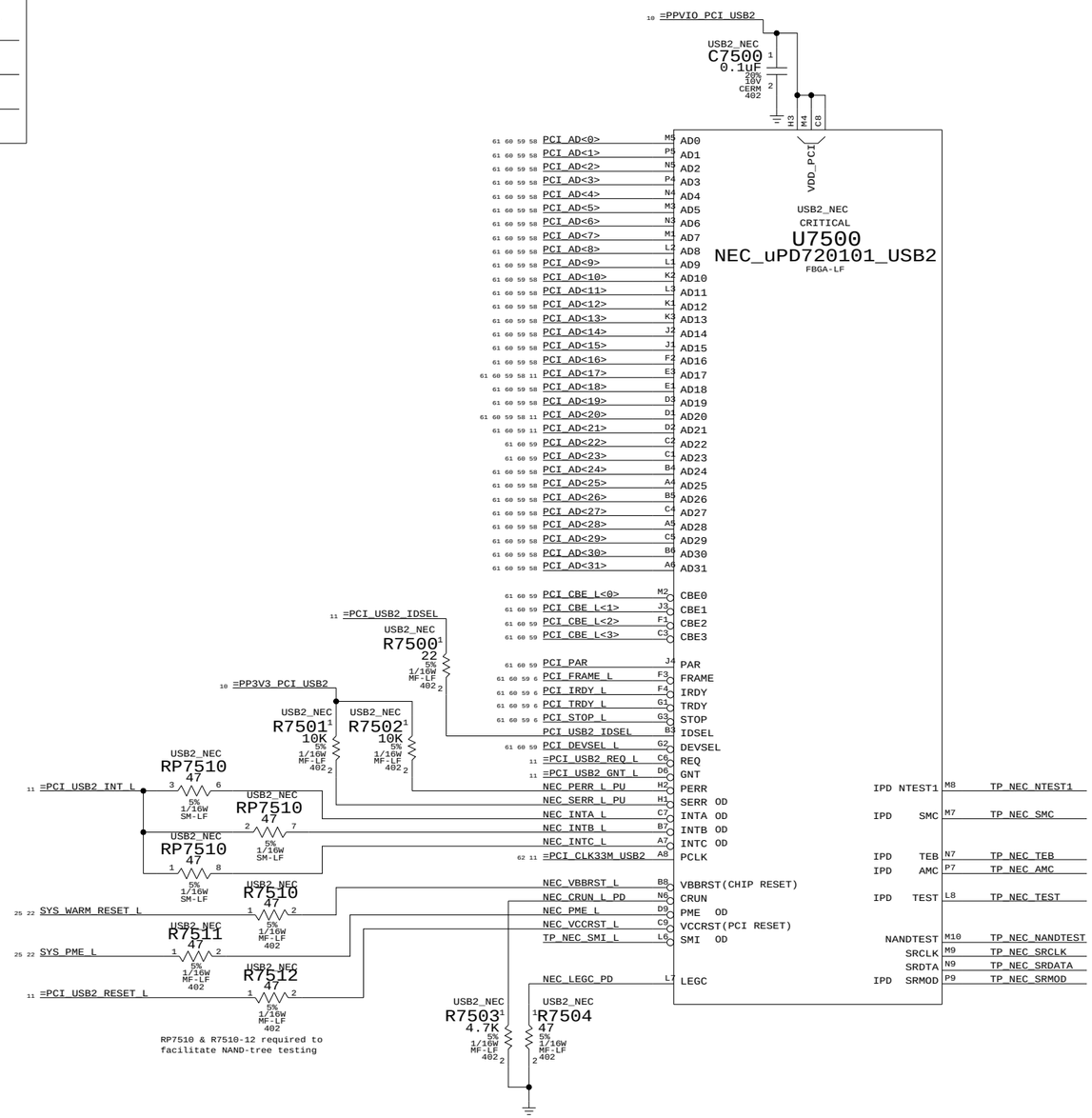
Power aliases required by this page:
- =PPVIO_PCI (to 3.3V or 5V)
- =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
- =PCI_CLK33M_USB2
- =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
- =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
- =PCI_USB2_INT_L

BOM options provided by this page:
- USB2_NEC

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.



NEC USB2

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 75 OF 115	

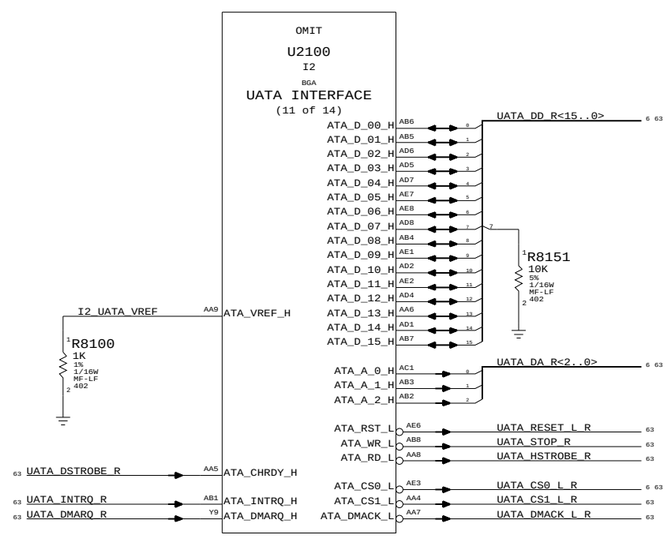
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
UATA_DD	UATA	UATA		UATA_DD_R<15..8>	6 63
UATA_DD7	UATA	UATA		UATA_DD_R<7>	6 63
UATA_DD	UATA	UATA		UATA_DD_R<6..0>	6 63
UATA_HOST	UATA	UATA		UATA_DA_R<2..0>	6 63
UATA_HOST	UATA	UATA		UATA_CS0_L_R	6 63
UATA_HOST	UATA	UATA		UATA_CS1_L_R	63
UATA_HSTROBE	UATA	UATA		UATA_HSTROBE_R	63
UATA_HOST	UATA	UATA		UATA_STOP_R	63
UATA_HOST_R	UATA	UATA		UATA_DMACK_L_R	63
UATA_HOST_R	UATA	UATA		UATA_RESET_L_R	63
UATA_DSTROBE	UATA	UATA		UATA_DSTROBE_R	63
UATA_DEV_R	UATA	UATA		UATA_DMARQ_R	63
UATA_DEV_R	UATA	UATA		UATA_INTRQ_R	63
	UATA	UATA		UATA_DD<15..0>	6 7 64
	UATA	UATA		UATA_DA<2..0>	6 7 64
	UATA	UATA		UATA_CS0_L	6 7 64
	UATA	UATA		UATA_CS1_L	7 63 64
	UATA	UATA		UATA_HSTROBE	7 63 64
	UATA	UATA		UATA_STOP	7 63 64
	UATA	UATA		UATA_DMACK_L	7 63 64
	UATA	UATA		UATA_RESET_L	7 63 64
	UATA	UATA		UATA_DSTROBE	7 63 64
	UATA	UATA		UATA_DMARQ	7 63 64
	UATA	UATA		UATA_INTRQ	7 63 64

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

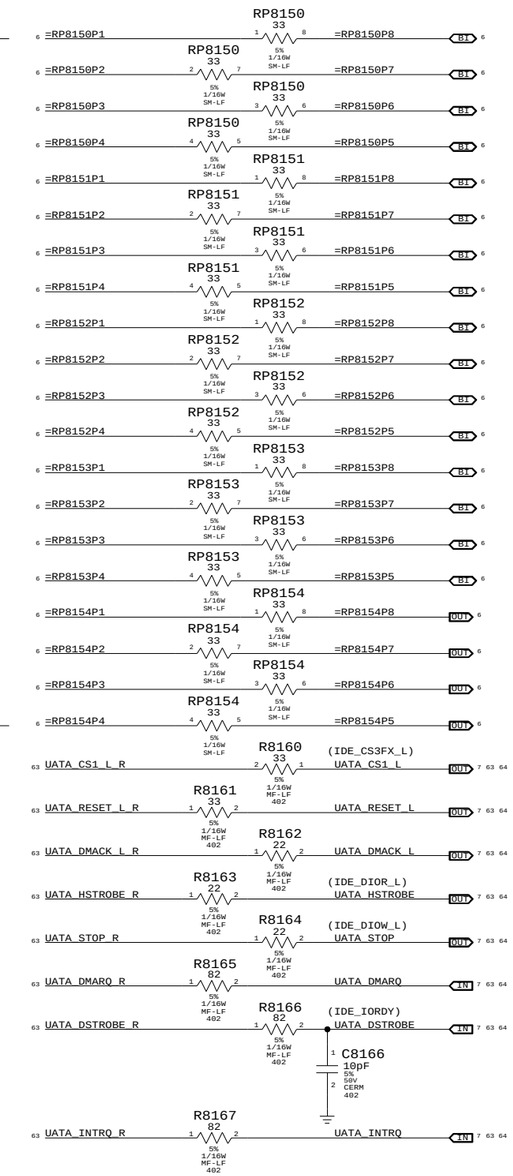
BOM options provided by this page:
(NONE)



UATA100 SERIES TERMINATION

PLACE CLOSE TO I2

One resistor for each of:
- UATA_DD<15..0>(_R)
- UATA_DA<2..0>(_R)
- UATA_CS0_L(_R)
(IDE_CS1FX_L)



I2 UATA Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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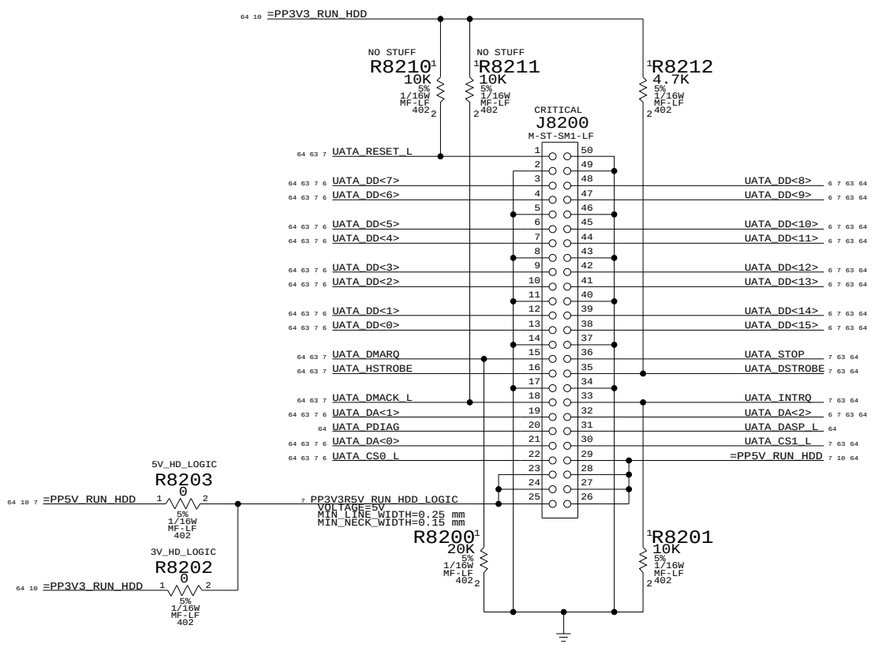
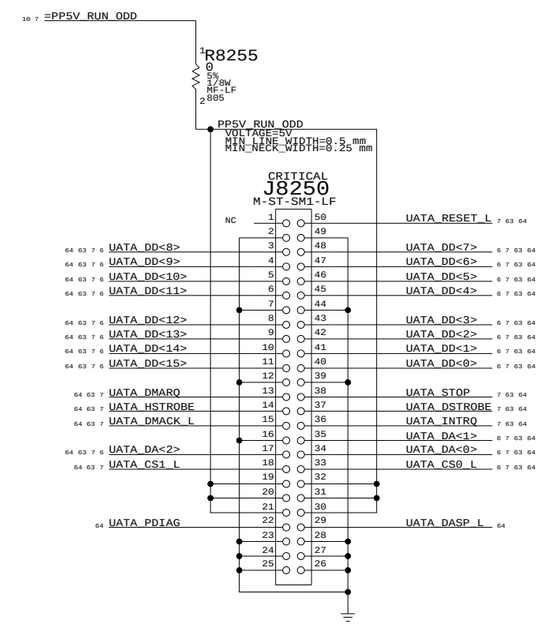
SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 81 OF 115	

HDD CONNECTOR



ODD CONNECTOR



ATA Connectors

Q16C/516S0357/M-ST-SM2-LF
Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 82 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
ENET_RX_CLK25M	CLOCK	CLOCK		ENET_CLK25M_TX	11 65
ENET_RX_CLK125M	CLOCK	CLOCK		ENET_CLK125M_RX	11 65
ENET_GBE_REF	CLOCK	CLOCK		ENET_CLK125M_GBE_REF	11 65
ENET_TX_CLK	CLOCK	CLOCK		ENET_CLK125M_GTX_R	65 66
ENET_RXD3_0	ENET	ENET		ENET_RXD<3..0>	9 11 65
ENET_RXD7_4	ENET	ENET		ENET_RXD<7..4>	9 11 65
ENET_RX_DV	ENET	ENET		ENET_RX_DV	9 11 65
ENET_RX_CTL	ENET	ENET		ENET_RX_ER	9 11 65
ENET_TXD3_0	ENET	ENET		ENET_TXD_R<3..0>	11 65
ENET_TXD7_4	ENET	ENET		ENET_TXD_R<7..4>	11 65
ENET_TX_EN	ENET	ENET		ENET_TX_EN_R	11 65
ENET_TX_ER	ENET	ENET		ENET_TX_ER_R	11 65
ENET_COL	ENET	ENET		ENET_COL	9 11 65
ENET_RX_CTL	ENET	ENET		ENET_CRS	9 11 65
ENET_MDC	ENET	ENET		ENET_MDC	9 11 65
ENET_MDIO	ENET	ENET		ENET_MDIO	9 11 65

Page Notes

Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

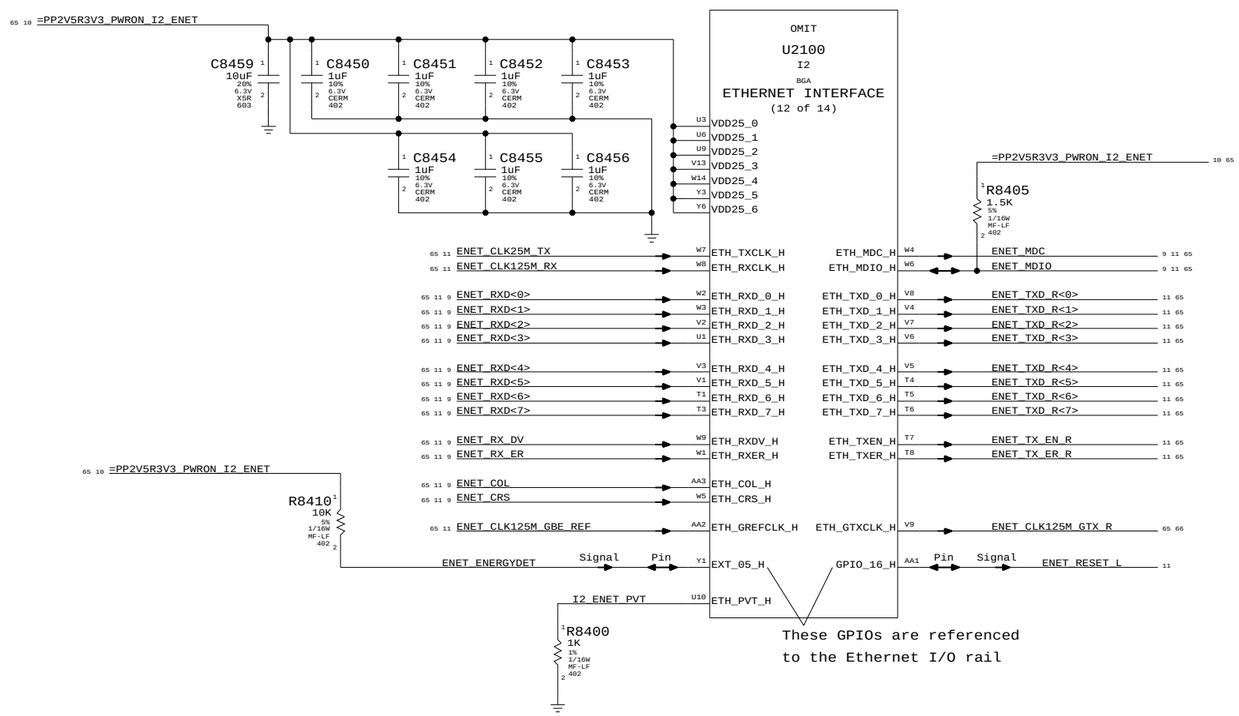
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



I2 Ethernet Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 84 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_GBE_REF_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_RX_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK25M_TX_R 66
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_N 66 67
VESTA_CLK25M_XTAL	XTAL	XTAL		VESTA_CLK25M_XTALI 66
	XTAL	XTAL		VESTA_CLK25M_XTALO 66
	XTAL	XTAL		VESTA_CLK25M_XTALO_R 66

Page Notes

Power aliases required by this page:
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

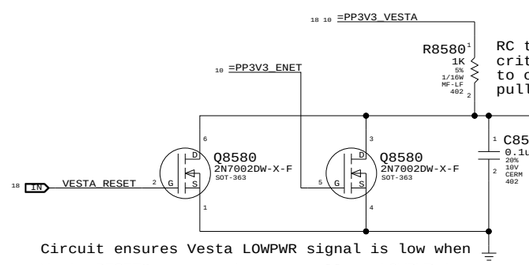
Net Spacing Type: ENET_MDI

~~Line To Line: 0.38 mms~~
~~Length Tolerance: 50 mils~~
~~Primary Max Sep: 5 mils~~
~~Secondary Max Sep: 100 mils~~
~~Secondary Length: 500 mils~~

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr

Disables Vesta Ethernet Circuit



RC time constant not critical. R < 3.9K to counter internal pulldown.

Circuit ensures Vesta LOWPWR signal is low when Vesta RESET* is asserted, and allows LOWPWR to assert when ethernet link is unpowered.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

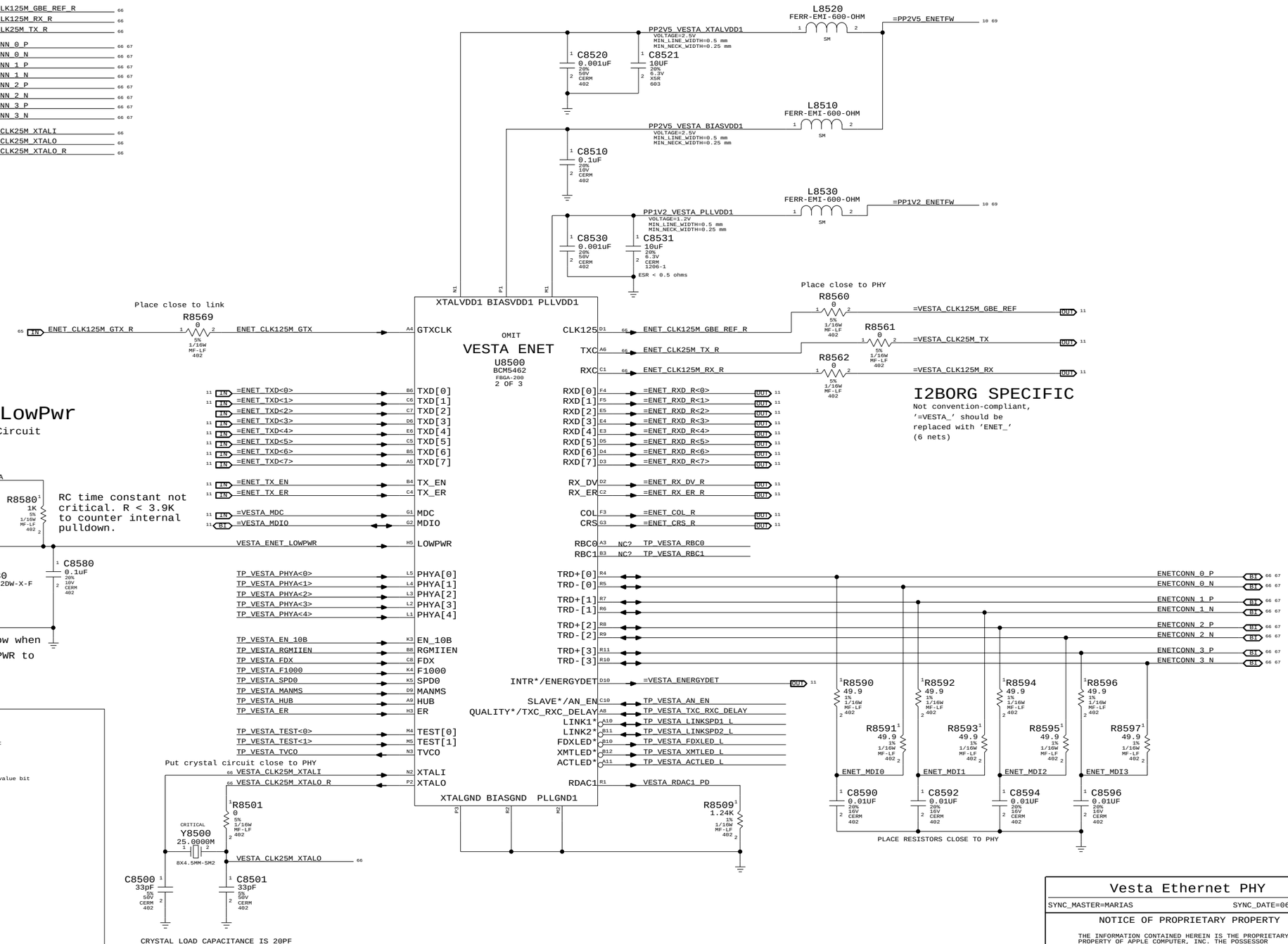
HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T



Vesta Ethernet PHY

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE NONE	SHT 85 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
PROVIDED BY ETHERNET PHY	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_P	67
	ENETCONN	ENETCONN	ENET_RJ45_0	ENETRJ45_0_N	67
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_P	67
	ENETCONN	ENETCONN	ENET_RJ45_1	ENETRJ45_1_N	67
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_P	67
	ENETCONN	ENETCONN	ENET_RJ45_2	ENETRJ45_2_N	67
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_P	67
	ENETCONN	ENETCONN	ENET_RJ45_3	ENETRJ45_3_N	67

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

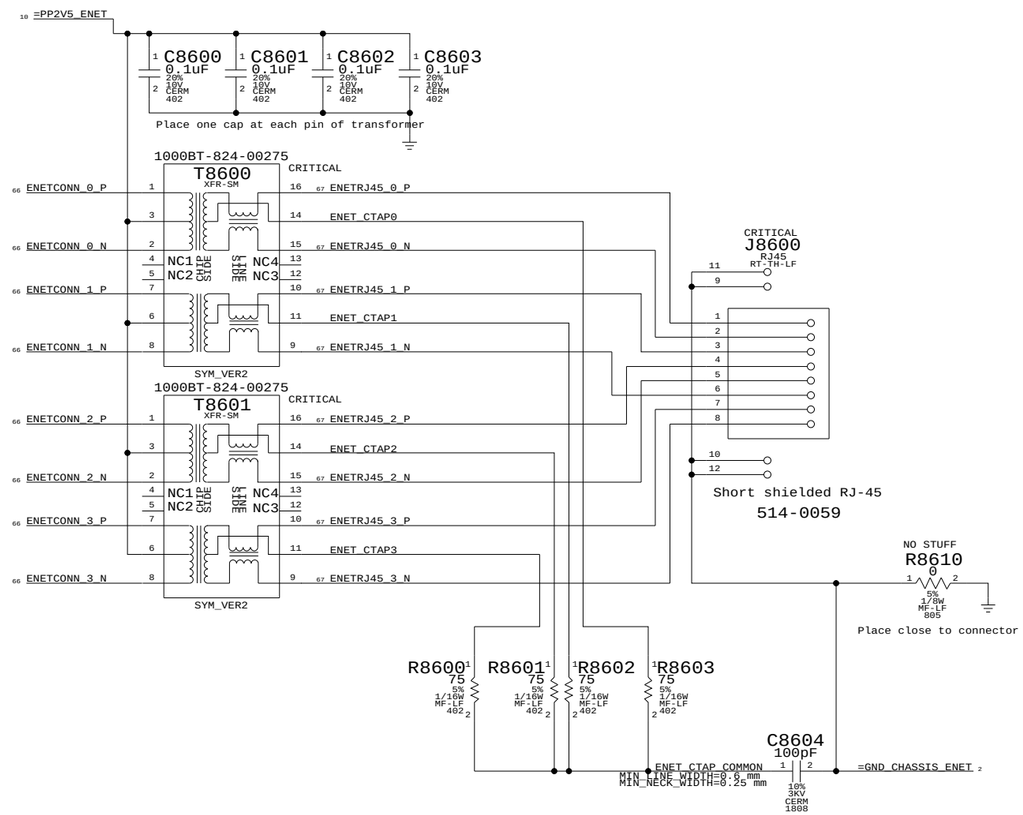
Sandwich each RJ54 pair between chassis grounds

Page Notes

Power aliases required by this page:
- _PP2V5_ENET
- _GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Transformers should be mirrored on opposite sides of the board

Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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D	051-6839	02
SCALE NONE	SHT 86 OF 115	

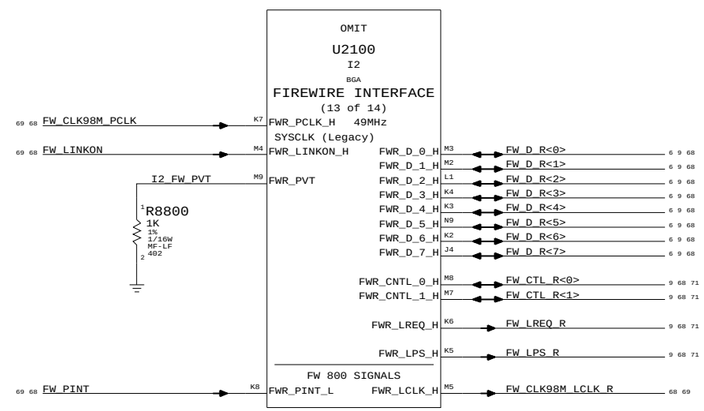
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FW_D_CTL	FW	FW		FW_D_R<7..0>	6 9 68
FW_D_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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D	051-6839	02
SCALE NONE	SHT 88 OF	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		FW_CLK98M_PCLK_R	69
	CLOCK	CLOCK		FW_CLK98M_LCLK	69
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_P	69 70
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_N	69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_P	69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_N	69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_P	69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_N	69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_P	69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_N	69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_P	69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_N	69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_P	69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_N	69 70
VESTA_CLK24M_XTAL	XTAL	XTAL		VESTA_CLK24M_XTALI	69
	XTAL	XTAL		VESTA_CLK24M_XTALO	69
	XTAL	XTAL		VESTA_CLK24M_XTALO_R	69

Page Notes

Power aliases required by this page:
- =PPFW_PHY_CPS
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

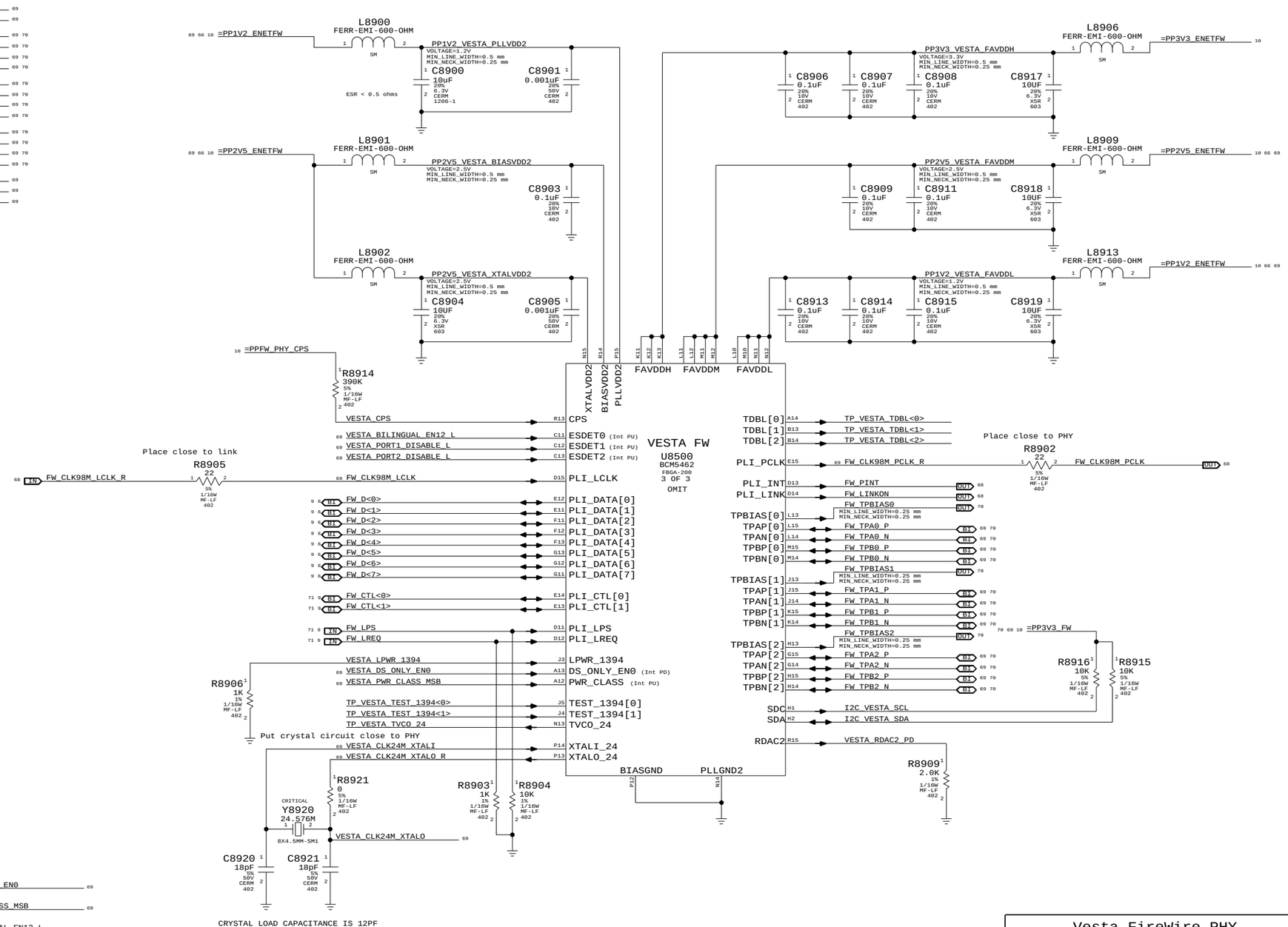
Signal aliases required by this page:
- NONE

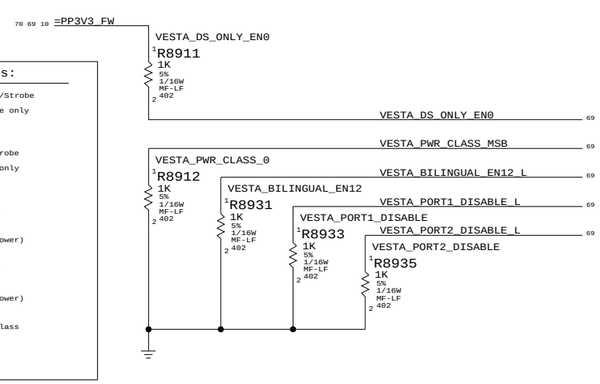
BOM options provided by this page:
- VESTA_BILINGUAL_EN12
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PORT1_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PORT2_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW_TP

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.





Vesta Config Straps:

DS_ONLY_EN12 - Port 1&2 Data/Strobe
1 - Port 1&2 Data/Strobe mode only
0 - Port 1&2 Bilingual mode
(Internal Pull-up)
DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)
PORT1_ENABLE - Port 1 Enable
1 - Port 1 Enabled
0 - Port 1 Disabled (saves power)
(Internal Pull-up)
PORT2_ENABLE - Port 2 Enable
1 - Port 2 Enabled
0 - Port 2 Disabled (saves power)
(Internal Pull-up)
PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

Vesta FireWire PHY

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 89 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
PROVIDED BY PHY PAGE	FW	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_P_FL
	FW	FW	FW_PORT1_TPA_FL	FW_PORT1_TPA_N_FL
	FW	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_P_FL
	FW	FW	FW_PORT1_TPB_FL	FW_PORT1_TPB_N_FL
	FW	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_P_FL
	FW	FW	FW_PORT2_TPA_FL	FW_PORT2_TPA_N_FL
	FW	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_P_FL
	FW	FW	FW_PORT2_TPB_FL	FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

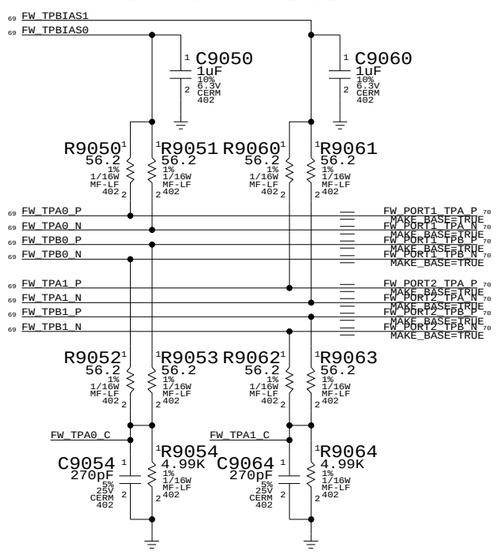
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

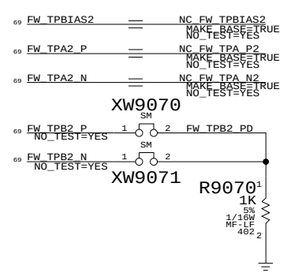
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

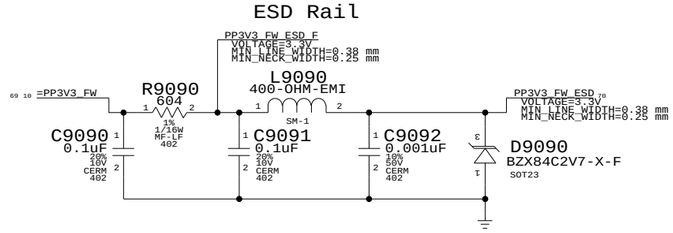
Place close to FireWire PHY



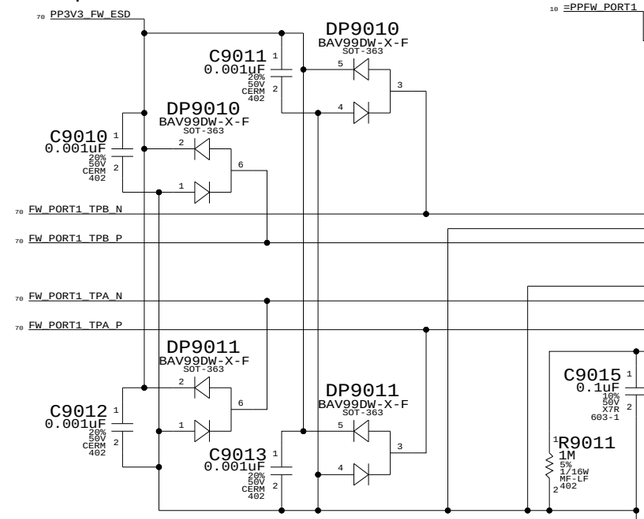
3rd TPA/TPB pair unused



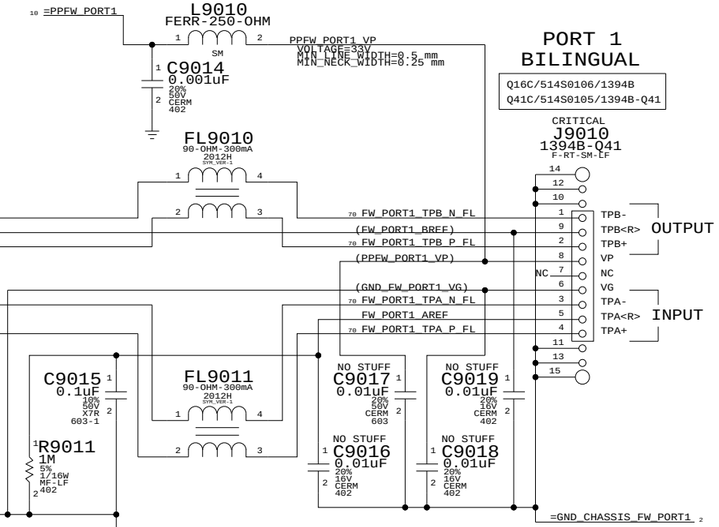
ESD Rail



"Snapback" & "Late VG" Protection



Cable Power

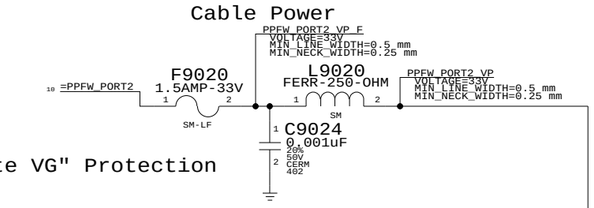


AREF needs to be isolated from all local grounds per 1394b spec

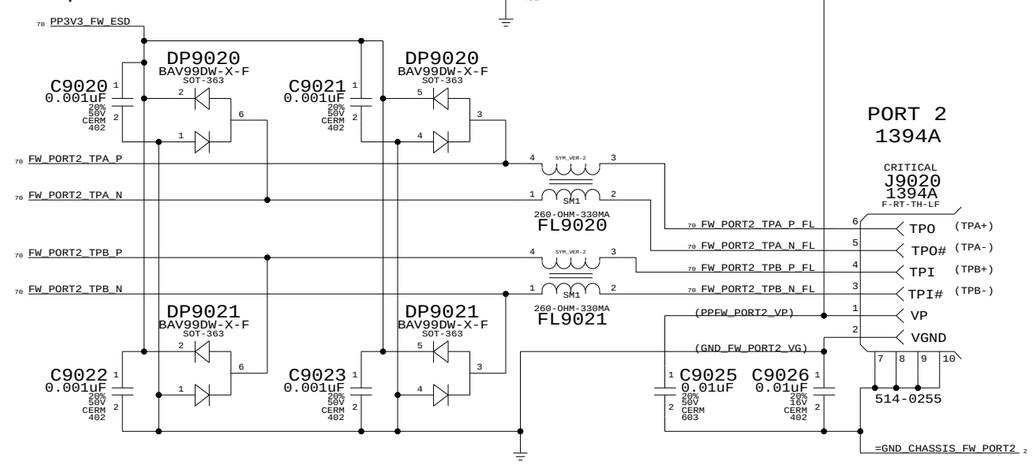
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

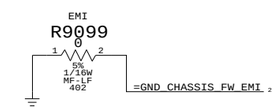
BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

Cable Power



"Snapback" & "Late VG" Protection





FireWire Ports

SYNC_MASTER=MARIAS-PDIFF SYNC_DATE=06/02/2005

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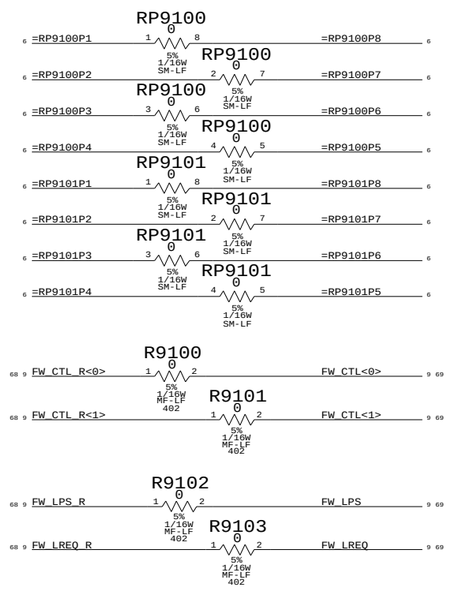
SCALE NONE	SHT 90 OF 115	

DRAWING
TITLE=PLASMA
ABBREV=DRAWING
LAST_MODIFIED=Fri Jun 3 15:18:37 2005

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.).



FireWire Series Term

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_P<0>	11 72
USB2_0	USB2	USB2	USB2_I2_0	USB2_I2_N<0>	11 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_P<1>	6 72
USB2_1	USB2	USB2	USB2_I2_1	USB2_I2_N<1>	6 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_P<2>	11 72
USB2_2	USB2	USB2	USB2_I2_2	USB2_I2_N<2>	11 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_P<3>	6 72
USB2_3	USB2	USB2	USB2_I2_3	USB2_I2_N<3>	6 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_P<4>	11 72
USB2_4	USB2	USB2	USB2_I2_4	USB2_I2_N<4>	11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_P<5>	11 72
USB2_5	USB2	USB2	USB2_I2_5	USB2_I2_N<5>	11 72
USB2_I2_XTAL	XTAL	XTAL		I2_CLK30M_USB2_XOUT_R	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XOUT	72
(USB2_I2_XTAL)	XTAL	XTAL		I2_CLK30M_USB2_XIN	72

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

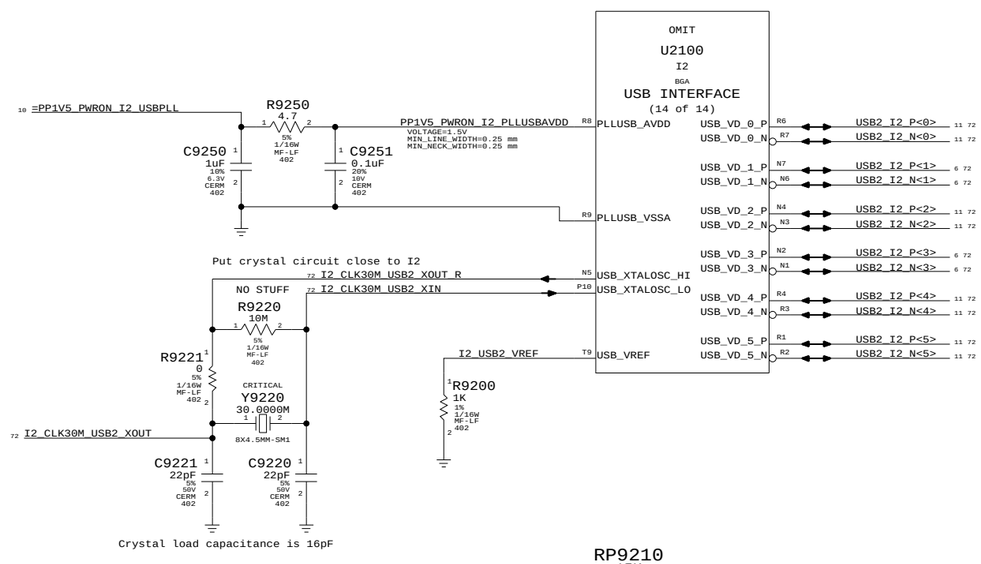
Signal aliases required by this page:
- =RP92xxPy (pinswappable USB pulldowns)

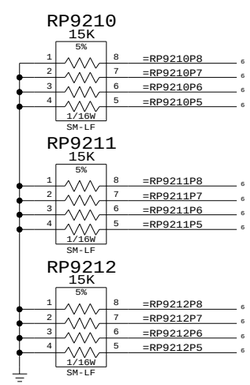
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

~~Line To Line:~~ 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary ~~Max Sep~~: 100 mils
~~Secondary~~ Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





One pair for each port USB2_*<0..5>

I2 USB Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SCALE NONE	SHT 92 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
ELECTRICAL_CONSTRAINT_SET (PROVIDED BY I2 PAGES)				
B30	USB2	USB2	USB2_NEC_0	USB2_NEC_P<0> 11 73
B31	USB2	USB2	USB2_NEC_0	USB2_NEC_N<0> 11 73
B32	USB2	USB2	USB2_NEC_1	USB2_NEC_P<1> 11 73
B33	USB2	USB2	USB2_NEC_1	USB2_NEC_N<1> 11 73
B34	USB2	USB2	USB2_NEC_2	USB2_NEC_P<2> 11 73
B35	USB2	USB2	USB2_NEC_2	USB2_NEC_N<2> 11 73
B36	USB2	USB2	USB2_NEC_3	USB2_NEC_P<3> 11 73
B37	USB2	USB2	USB2_NEC_3	USB2_NEC_N<3> 11 73
B40 USB2_NEC_XTAL	XTAL	XTAL		NEC_CLK30M_XT1 73
B41	XTAL	XTAL		NEC_CLK30M_XT2 73
B42	XTAL	XTAL		NEC_CLK30M_XT2_R 73

Page Notes

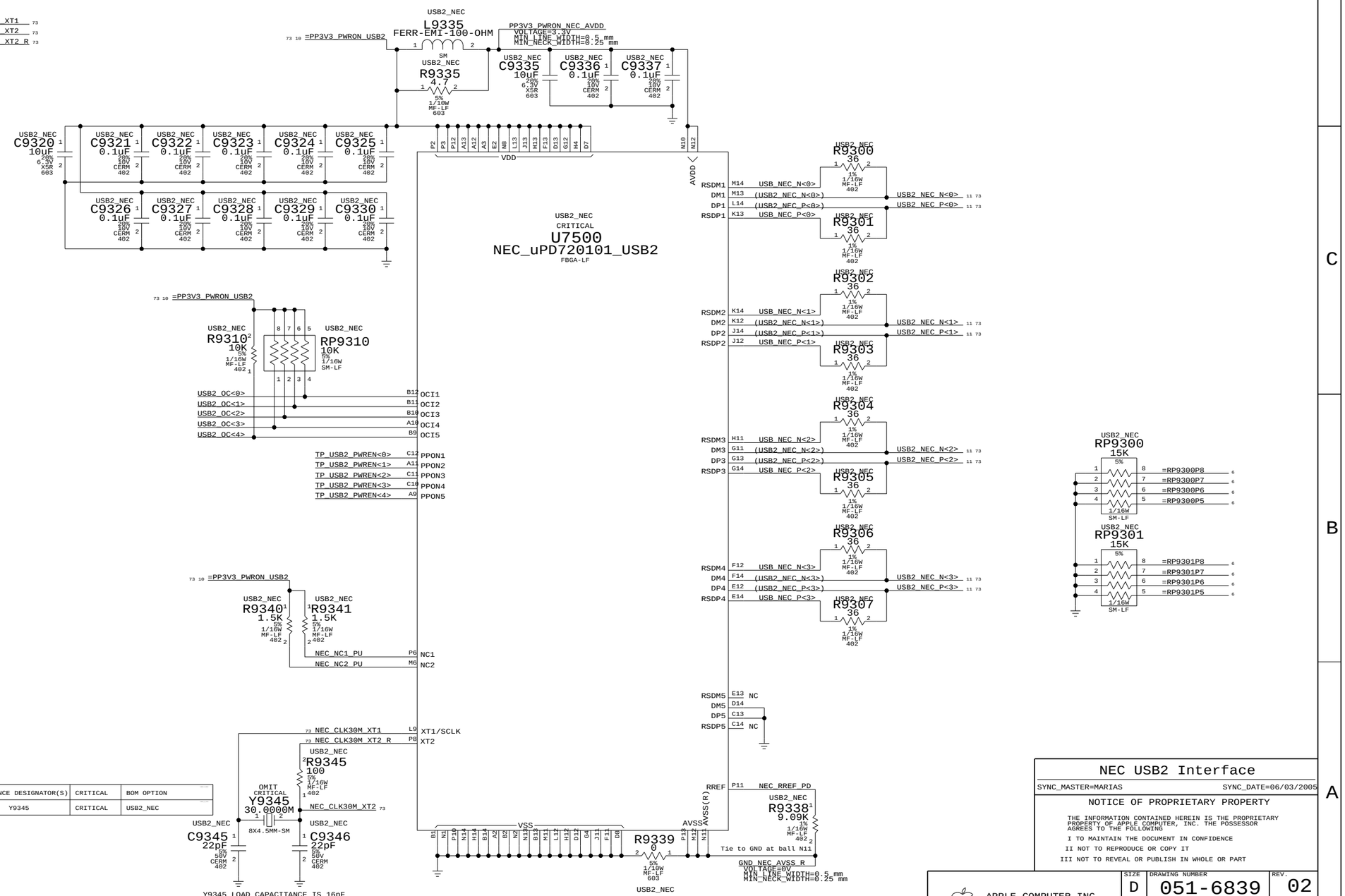
Power aliases required by this page:
- =PP3V3_PWRON_USB2

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,30.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC

NEC USB2 Interface

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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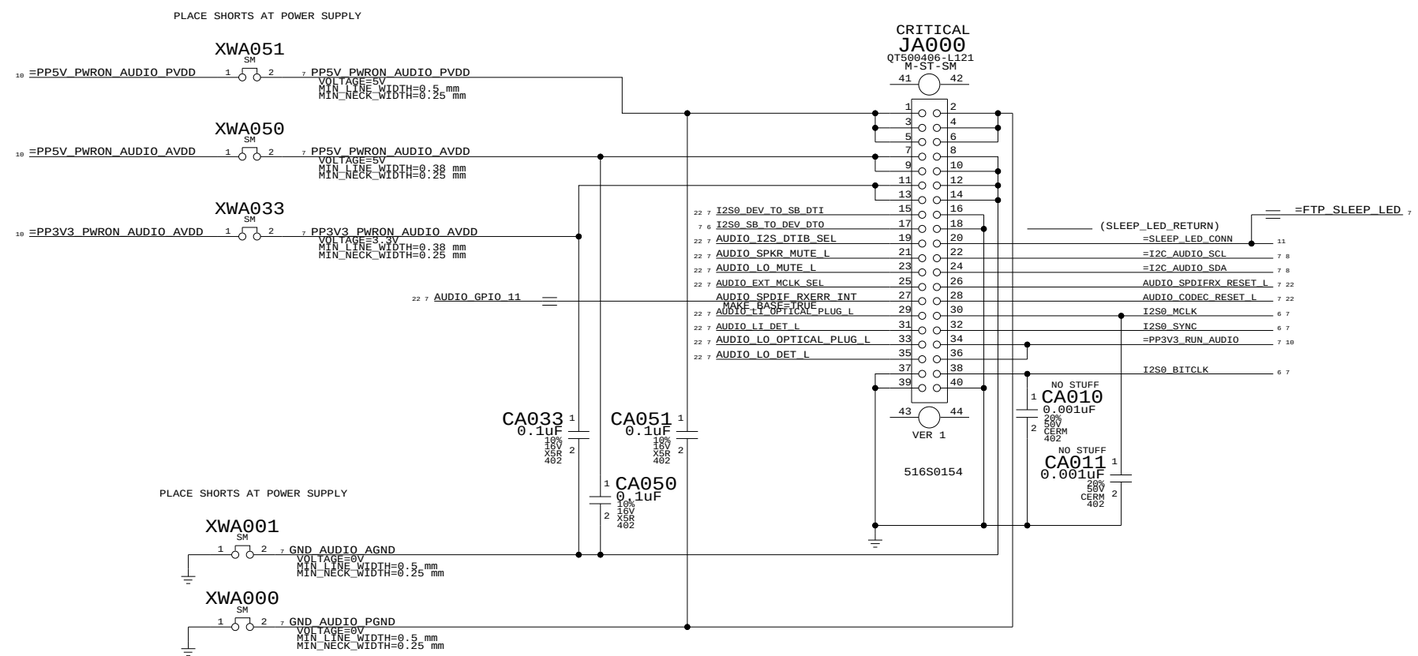
SCALE NONE SHT 93 OF 115

AUDIO BOARD CONNECTOR

Place all shorts at output of 3.3V and 5V regulator



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 100 OF 115	

AGP

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     AGP          401          *          0.4 MM         =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_SPACING_RULE
     AGP_STB      601          *          0.6 MM          2.5 MM          =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     AGP                *         =STANDARD         =60_OHM_SE         =60_OHM_SE         =60_OHM_SE
TABLE_PHYSICAL_RULE
     AGP_STB            *         =STANDARD       =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
```

CLOCK

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     CLOCK        251          *          0.25 MM        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     CLOCK              *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

ENET (Ethernet Digital)

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     ENET_SELF    =STANDARD    *         =STANDARD        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_SPACING_RULE
     ENET         201          *          0.2 MM         =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     ENET               *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     ENET                ENET                *           ENET_SELF
```

FW (FireWire Digital)

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     FW_SELF      =STANDARD    *         =STANDARD        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_SPACING_RULE
     FW           201          *          0.2 MM         =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     FW                 *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     FW                  FW                  *           FW_SELF
```

I2C

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     I2C          201          *          0.2 MM         =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     I2C                *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

MaxBus

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     MAXBUS       151          *          0.15 MM        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     MAXBUS             *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

PCI

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     PCI          =STANDARD    *         =STANDARD        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     PCI                *         =STANDARD         =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

RAM

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     RAM          201          *          0.2 MM         =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_SPACING_RULE
     RAM_DIFF     251          *          0.25 MM         2.5 MM          =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     RAM                *         =50_OHM_SE        =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
TABLE_PHYSICAL_RULE
     RAM_DIFF           *       =100_OHM_DIFF     =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
```

UATA

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     UATA         151          *          0.15 MM        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     UATA               *         =50_OHM_SE        =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

USB2

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     USB2         501          *          0.50 MM         3.81 MM          =90_OHM_DIFF       =90_OHM_DIFF       =90_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     USB2               *         =90_OHM_DIFF      =90_OHM_DIFF       =90_OHM_DIFF       =90_OHM_DIFF
```

AUDIO

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     AUDIO        251          *          0.25 MM        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     AUDIO              *         =50_OHM_SE        =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

I2S

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     I2S          251          *          0.25 MM        =STANDARD          =STANDARD          =STANDARD          =STANDARD
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     I2S                *         =50_OHM_SE        =50_OHM_SE         =50_OHM_SE         =50_OHM_SE
```

ENETCONN

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     ENETCONN     501          *          0.50 MM         3.81 MM          =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     ENETCONN           *       =100_OHM_DIFF     =100_OHM_DIFF      =100_OHM_DIFF      =100_OHM_DIFF
```

FW_TP

```
TABLE_SPACING_RULE
TABLE_SPACING_RULE
     FW_TP        501          *          0.50 MM         3.81 MM          =110_OHM_DIFF      =110_OHM_DIFF      =110_OHM_DIFF
TABLE_PHYSICAL_RULE
TABLE_PHYSICAL_RULE
     FW_TP              *       =110_OHM_DIFF     =110_OHM_DIFF      =110_OHM_DIFF      =110_OHM_DIFF
```

I2_FBCLK / XTAL

```
TABLE_SPACING_ASSIGNMENT
TABLE_SPACING_ASSIGNMENT
     I2_FBCLK           *                 *             CLOCK
TABLE_SPACING_ASSIGNMENT
     XTAL               *                 *             CLOCK
TABLE_PHYSICAL_ASSIGNMENT
TABLE_PHYSICAL_ASSIGNMENT
     I2_FBCLK           *             CLOCK
TABLE_PHYSICAL_ASSIGNMENT
     XTAL               *             CLOCK
```

Spacing & Physical Constraints

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
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DVO

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
DVO	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE		

S-VIDEO

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE							
TV_CONN	151	*	=TV	=TV	=TV	=TV	=TV
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
TV	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE		
TABLE_PHYSICAL_RULE							
TV_CONN	*	=TV	=TV	=TV	=TV		

VGA

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE
TABLE_SPACING_RULE							
VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA	=VGA
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
VGA	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE		
TABLE_PHYSICAL_RULE							
VGA_CONN	*	=VGA	=VGA	=VGA	=VGA		

LVDS

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
LVDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF		

TMDS

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_SPACING_RULE							
TMDS_CONN	=TMDS	*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
TMDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF		
TABLE_PHYSICAL_RULE							
TMDS_CONN	*	=TMDS	=TMDS	=TMDS	=TMDS		

THERM

TABLE_SPACING_RULE							
TABLE_SPACING_RULE							
THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TABLE_PHYSICAL_RULE							
TABLE_PHYSICAL_RULE							
THERM	*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF		

Spacing & Physical Constraints 2

SYNC_MASTER=MARIAS SYNC_DATE=06/03/2005

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SIZE	DRAWING NUMBER	REV.
D	051-6839	02

SCALE NONE SHT 111 OF 115

```
*** Signal Cross-Reference for the entire design ***

1V5RUN_EN          16A6<> 26C6<
1V8RUN_EN_L        16A4<> 26B4<>
1V8_1V5PWRON_EN_L  26D4<
1V20_REF           12C7< 14C8<
1V65_REF           13A5<
1_5V_BOOST         16C6<>
1_5V_BST           16C5<>
1_5V_DH            16C6<>
1_5V_DL            16B6<>
1_5V_FB            16B7<
1_5V_ILIM          16C5<>
1_5V_LX            16B5<>
1_8V_BOOST         16C4<>
1_8V_BST           16C4<>
1_8V_DH            16C3<>
1_8V_DL            16B3<>
1_8V_FB            16B4<
1_8V_ILIM          16C5<>
1_8V_LX            16B3<>
1_8V_PVDD_STD      51C1<
2V5PWRON_EN_L      26D4<
2V5RUN_EN_L        17A5<> 26C6<
3V3RUN_EN_L        15B3<> 26C5<
3V_BG              15C4<>
3V_BOOST           15C4<>
3V_BOOST_ESR       15D3<>
3V_ITH             15C4<>
3V_ITH_RC          15C3<
3V_PMU_VTAP        14B3<
3V_RSNS            15D2<
3V_RUNSS           15C4<
3V_SNSM            15C4<
3V_SNSP            15C4<
3V_SW              15C4<>
3V_TG              15D4<>
3V_VOSNS           15C4<>
5V3V3PWRON_EN_L  26D6<
5V3VPWRON_EN_L_RC  15B6<
5VRUNHD_EN_L       15B5<> 26D5<
5VRUN_EN_L         15A5<> 26D5<
5VTPAD_EN_L        26B5<
5V_BG              15C5<>
5V_BOOST           15C5<>
5V_BOOST_ESR       15D6<>
5V_ITH             15C5<>
5V_ITH_RC          15C6<
5V_RSNS            15D7<
5V_RUNSS           15C5<
5V_SNSM            15C5<
5V_SNSP            15C5<
5V_SW              15C5<>
5V_TG              15C5<>
5V_VOSNS           15C5<>
1625_BG            14C5<>
1625_BST           14C5<
1625_BST_ESR       14C5<>
1625_COMP          13D2< 14C6<
1625_DIV           14C8<
1625_ENABLE        14D7<>
1625_ENABLE_L      14D7<>
1625_FCB           14C6<
1625_INTVCC        14C5<>
1625_RUNSS         14C6<
1625_SGND          14B7<>
1625_TG            14C5<>
1625_VFB           14B5<>
1625_VIN           14C6<
1625_VSW           14C4<>
1772_ACIN          13B5<
1772_ACOK_L        13B5<> 13C4<>
1772_BST           13B4<>
1772_BST_ESR       13C3<
1772_CCI           13B5<>
1772_CCS           13B5<
1772_CCV           13B5<>
1772_CCV_RC        13B5<
1772_CELLS         13B4<
1772_CLS           13A4<
1772_CSIN          13B4<>
1772_CSIP          13B4<>
1772_CSSN          13C5<
1772_CSSP          13C5<
1772_DCIN          13B5<
1772_DHI           13B4<>
1772_DLO           13B4<>
1772_DLOV          13B4<>
1772_GND           13A5<>
1772_ICHG          13B5<>
1772_ICTL          13B5<>
1772_IINP          13B5<
1772_LDO           13C4<>
1772_LX            13B4<>
1772_REF           13B5<>
1772_VCTL          13B5<
1778_BG            45C5<>
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1778_ION           45C5<
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1778_VRNG          45C6<
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3707_FSET          15C5<
3707_INTVCC        15D5<>
3707_SGND          15C7<>
3707_STBYMD        15C5<>
=1V8_1V5PWRON_EN_L  16C8<> 26D3>
=1V8_1V5PWRON_PGOOD  16C6> 26B8<
=2V5PWRON_EN_L   17C7<> 26D3>
=2V5PWRON_PGOOD  17C4> 26B8<
=5V3V3PWRON_EN_L  15B6< 26D5>
=5V3VPWRON_PGOOD  15C4<> 26B8<
=5VPWRONTPAD_EN_L  15A8<> 26B4>
=ADT7467_THERM_L  11B3> 27C2<
=AGP_GPU_RESET_L  11C7> 44D4<
=AGP_VREF          11C7> 44B2<
=CLK33M_TBEN_SYNC  11D1> 21A5< 21D6>
=CPU0_MAX1717_AB_SEL  11A3> 36A7< 36C7<
=CPU0_VID_AB_SEL  11A3> 36D3<>
=CPU_HRESET_L      11B3> 34A8< 34C6< 34D4<
=ENET_COL_R        11A6> 66B3>
=ENET_CRS_R        11A6> 66B3>
=ENET_RXD_R<0>     66C3>
=ENET_RXD_R<7..0>  11A6>
=ENET_RXD_R<1>     66C3>
=ENET_RXD_R<2>     66C3>
=ENET_RXD_R<3>     66C3>
=ENET_RXD_R<4>     66C3>
=ENET_RXD_R<5>     66C3>
=ENET_RXD_R<6>     66C3>
=ENET_RXD_R<7>     66C3>
=ENET_RX_DV_R      11A6> 66C3>
=ENET_RX_ER_R      11A6> 66B3>
=ENET_TXD<0>       66C6<
=ENET_TXD<7..0>    11A6>
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=ENET_TXD<7>       66C6<
=ENET_TX_EN        11A6> 66C6<
=ENET_TX_ER        11A6> 66B6<
=FTP_GND           7C5> 7C5> 7C7> 10D2>
=FTP_SLEEP_LED     7C5> 74C2>
=FWPWR_PWRON       18C8<> 26D3>
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=GND_CHASSIS_DVI2  2D4> 57C3<>
=GND_CHASSIS_DVI3  2D4> 57C2<
=GND_CHASSIS_DVI4  2D4> 57B2<
=GND_CHASSIS_DVI_HOLE  2D2<> 2D4>
=GND_CHASSIS_ENET  2D4> 67A3<>
=GND_CHASSIS_FW_EMI  2D4> 70A1<
=GND_CHASSIS_FW_HOLE  2D1<> 2D4>
=GND_CHASSIS_FW_PORT1  2D4> 70C1<>
=GND_CHASSIS_FW_PORT2  2D4> 70A2<>
=GND_CHASSIS_INVERTER1  2C4> 56B3<
=GND_CHASSIS_INVERTER2  2C4> 56A2<
=GND_CHASSIS_INV_GND_CLIP  2D1<> 2D4>
=GND_CHASSIS_LCD1  2D4> 56C5<>
=GND_CHASSIS_LCD2  2D4> 56C6<

=GND_CHASSIS_LCD3  2D4> 56B6<
=GND_CHASSIS_LCD4  2D4> 56A5<>
=GND_CHASSIS_SVIDEO_HOLE  2D1<> 2D4>
=GND_CHASSIS_TV  2D4> 57A7<>
=GPUVCORE_PGOOD  26A8< 45C6>
=GPU_AGP_VREF     11C7> 44B4<
=I2C_ADT7467_SCL  8B1> 27C4<
=I2C_ADT7467_SDA  8B1> 27C4<>
=I2C_AUDIO_SCL   7A7> 8D1> 74B3<>
=I2C_AUDIO_SDA   7A7> 8D1> 74B3<>
=I2C_BATT_SCL    8B4> 12A5<
=I2C_BATT_SDA    8B4> 12A5<
=I2C_DS1775_SCL  7C5> 8B1> 30C6<>
=I2C_DS1775_SDA  7C5> 8B1> 30C6<>
=I2C_GPU_TMDS_SCL  8A5< 51B3<>
=I2C_GPU_TMDS_SDA  8A5< 51B3<>
=I2C_I2_NB_SCL   8C3< 22C2<
=I2C_I2_NB_SDA   8C3< 22C2<
=I2C_I2_SB_SCL   8D3< 22C2<
=I2C_I2_SB_SDA   8D3< 22B2<
=I2C_PMU_SCL     8C5< 25C5<>
=I2C_PMU_SDA     8C5< 25C5<>
=I2C_PMU_SMB_SCL  8B5< 25C5<>
=I2C_PMU_SMB_SDA  8B5< 25C5<>
=I2C_SI_M_SCL    8A4> 54B6<
=I2C_SI_M_SDA    8A4> 54B6<
=I2C_SI_S_SCL    8A4> 55B6<
=I2C_SI_S_SDA    8A4> 55B6<
=I2C_SODIMM_SCL  8C1> 40A6<> 41A6<>
=I2C_SODIMM_SDA  8C1> 40A6<> 41A6<>
=I2VCORE_PGOOD   20C4> 26B8<
=I2_AGP_FBCLK_IN  21C5> 43A5<
=I2_AGP_VREF      11C7> 43B5<
=I2_MAXBUS_FBCLK_IN  21D1> 32A6<
=I2_PCI_FBCLK_IN  21B5> 59A5<
=I2_STOPCPU_L     11B3> 22A5<
=I2_STOPXTAL_L    11B3> 22A5<
=JTAG_BBANGER_TCK  9D8< 25B5<>
=JTAG_BBANGER_TDI  9D8< 25B5<>
=JTAG_BBANGER_TMS  9D8< 25B5<>
=JTAG_BBANGER_TRST_L  9D8< 25C5<>
=JTAG_CPU0_TCK    9D5> 34D6<
=JTAG_CPU0_TDI    9D6> 34D6<
=JTAG_CPU0_TDO    9D6< 34D6<
=JTAG_CPU0_TMS    9D5> 34D6<
=JTAG_CPU0_TRST_L  9D5> 34D6<
=JTAG_I2_TCK      9B6> 22B5<
=JTAG_I2_TDI      9C6> 22B5<
=JTAG_I2_TDO      9C6< 22B2<
=JTAG_I2_TMS      9B6> 22B5<
=JTAG_I2_TRST_L   9B6> 22A5<
=JTAG_VESTA_TCK   9A6> 18A6<
=JTAG_VESTA_TDI   9A6> 18A6<
=JTAG_VESTA_TDO   9A6< 18A6<
=JTAG_VESTA_TMS   9A6> 18A6<
=JTAG_VESTA_TRST_L  9A6> 18A6<
=MAXBUS_CPU0_CLK  11D4> 33C1< 33D6>
=PCI_AIRPORT_GNT_L  11D1> 60C3<>
=PCI_AIRPORT_IDSEL  11C1> 60C7<
=PCI_AIRPORT_INT_L  11C1< 60B3<>
=PCI_AIRPORT_REQ_L  11D1> 60C5<>
=PCI_AIRPORT_RESET_L  11C1> 60C3<>
=PCI_CBUS_GNT_L  11C1> 61A7<
=PCI_CBUS_IDSEL  11C1> 61B8<
=PCI_CBUS_INT_L  11C1< 61A7<>
=PCI_CBUS_REQ_L  11C1> 61A7<
=PCI_CBUS_RESET_L  11C1> 61A7<
=PCI_CLK33M_AIRPORT  11D1> 60B5<> 60D6>
=PCI_CLK33M_CBUS  11C1> 61A7< 61D1>
=PCI_CLK33M_USB2  11C1> 62B5< 62D6>
=PCI_CLK33M_ZDBOUT_R<0>  11D4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<1>  11C4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<2>  11C4< 23B4> 23D6>
=PCI_CLK33M_ZDBOUT_R<3>  11B4< 23B4> 23D6>
=PCI_CLK33M_ZDB_IN  11D1> 23B5< 23D6>
=PCI_USB2_GNT_L  11C1> 62B5<
=PCI_USB2_IDSEL  11B1> 62B6<
=PCI_USB2_INT_L  11B1> 62B7<
=PCI_USB2_REQ_L  11C1> 62B5<
=PCI_USB2_RESET_L  11B1> 62A7<
=PP1V2_ENETFW    10D4> 66D2< 69C1< 69D5<
=PP1V2_VESTA     10D4> 18B7<
=PP1V2_VESTA_REG  10D6> 18C1<
=PP1V05R1V3_GPU_VCORE  10A6> 46D6<
=PP1V5R1V8_I2_MAXBUS  10A1> 32B6< 32D1<
=PP1V5R1V8_MAXBUS  10A1> 21C8< 33A5< 33B8< 33C8<
            34B5< 34B7< 34C4< 34C4< 34D4<
=PP1V5R3V3_DVO_VREF  47C1> 54A2<
=PP1V5_AGP        10A6> 43A5< 43C1< 44B2< 44B7<
            44C6< 47C2<
=PP1V5_GPU        10A1> 10A8<
=PP1V5_GPU_DVO    10A6> 47C2<
=PP1V5_GPU_PWRSEQ  10A6> 52C4<>
=PP1V5_GPU_VDD15  10A6> 46B5<>
=PP1V5_I2_AGP     10A4> 43C7<
=PP1V5_PWRON_I2PLL_LDO  10D3< 20B3<>
=PP1V5_PWRON_I2_PLL  10D1> 19C5<
=PP1V5_PWRON_I2_USBPLL  10D1> 72C7<
=PP1V5_PWRON_REG  10A6<> 16B8<>
=PP1V5_PWRON_RUNFET  10A4> 16A8<>
=PP1V5_RUN_RUNFET  10A3< 16A6<>
=PP1V8R2V5_GPU_FB_VIO  10A6> 47C8< 48A8<
=PP1V8_FB_VDD     10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_FB_VDDQ    10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_GPU        10A1> 10A8<
=PP1V8_GPU_AVDD   10A8< 53C2<
=PP1V8_GPU_DVO    10A6> 47C2<
=PP1V8_GPU_LVDS_PLL  47C2< 51D1>
=PP1V8_GPU_MEMVMODE  10A6> 48A6<
=PP1V8_GPU_PANEL_IO  10A6> 47B2<
=PP1V8_GPU_PWRSEQ  10A6> 52D4<>
=PP1V8_GPU_TPVDD  10A8< 53D4<
=PP1V8_PWRON_DDR2  10A4> 40B8< 40C3< 40D4<> 40D6<>
            41C3< 41D4<> 41D6<>
=PP1V8_PWRON_I2_RAM  10A4> 38D3<
=PP1V8_PWRON_REG  10A6<> 16C1<>
=PP1V8_PWRON_RUNFET  10A4> 16B5<>
=PP1V8_RAM_I2_VREF  10A1> 38A6<
=PP1V8_RUN_RUNFET  10A3< 16A3<>
=PP1V8_RUN_TBEN_SYNC  10A1> 21B5<
=PP2V5R3V3_PWRON_I2_ENET  10B5< 65B6< 65C3< 65C7<
=PP2V5_ENET       10A4> 67C6<>
=PP2V5_ENETFW     10D4> 66D2< 69D1< 69D5<
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=PP2V5_GPU_A2VDD  10A6> 53B2<
=PP2V5_GPU_LVDS_IO  10B6> 47B1<
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=PP2V5_PWRON_REG  10A6<> 17C2<
=PP2V5_PWRON_RUNFET  10A4> 17B5<>
=PP2V5_RUN_PCI1510  10B1> 61C8<
=PP2V5_RUN_RUNFET  10B3< 17B4<>
=PP2V5_VESTA      10D4> 18B2<
=PP2V5_VESTA_LDO  10D6< 18D1<>
=PP2V7R5V5_PWRON_I2VCORE  10B4> 20D7<
=PP2V8_GPU_LVDDR_LDO  10B8> 52B1<>
=PP2V8_GPU_LVDS_IO  10B6> 47A1<
=PP3V3_ADT7467    10B4> 27D5<
=PP3V3_AGP        10B6> 43D1< 44B4< 44C7<
=PP3V3_ALL_A29_DET  10C6> 12D3<>
=PP3V3_ALL_AC_DETECT  10C6> 12C7<>
=PP3V3_ALL_BATT0_DET  10B6> 12B7<
=PP3V3_ALL_BATT_CHGR  10C6> 13A6<> 13A8< 13C8<
=PP3V3_ALL_DEBUG  10B6> 24C3<>
=PP3V3_ALL_HALL_EFFECT  10C6> 30D6<
=PP3V3_ALL_LTC1625_SW  10C6> 14C7<>
=PP3V3_ALL_PBUS_ILIM  10C6> 13C3< 13D4<
=PP3V3_ALL_PMU    10C6> 24A7< 24D7< 25B6< 25B8<
            25D5<
=PP3V3_ALL_PWRSEQ  10B6> 26D5<
=PP3V3_ALL_VREG  10C8< 14A2<
=PP3V3_BATT_IMON  10B6> 12A5<
=PP3V3_DDC_DVI   10B1> 57B4<> 57D2<>
=PP3V3_DDC_LCD   7B7> 10B1> 56C7<>
=PP3V3_ENET       10A5< 66B7<>
=PP3V3_ENETFW     10D4> 69D1<
=PP3V3_FW         10D4> 69A8< 69B2< 70A8<
=PP3V3_GPU        10B1> 10B8<
=PP3V3_GPU_CLOCKS  10B1> 52B8< 52C8<
=PP3V3_GPU_GPIOS  10B6> 51A7< 51B8< 53C4<
=PP3V3_GPU_PWRSEQ  10B6> 52D2<>
=PP3V3_GPU_VDDR3  10B6> 47D3<
=PP3V3_I2_PCISLOTEGPIOS  10B5< 22B7<
=PP3V3_PCI        10B1> 59D1<
=PP3V3_PCI_AIRPORT  10B1> 60C3<>
=PP3V3_PCI_ROM   10B5< 58B6< 58C5<>
=PP3V3_PCI_USB2  10B3< 62B6<
=PP3V3_PCI_ZDB   10B3< 23C5<

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=PP3V3_PWRON_BT  10B4> 60C6<>
=PP3V3_PWRON_CPUVCORE_OFFSET  10B3> 36B7<
=PP3V3_PWRON_CPUVCORE_VID  10B4> 36C8< 36D6<
=PP3V3_PWRON_DS1775  10B4> 30D6<
=PP3V3_PWRON_I2_AGPPCI  10B5< 19A5<
=PP3V3_PWRON_I2_IO1  10B5< 19C5<
=PP3V3_PWRON_I2_IO2  10B5< 19B5<
=PP3V3_PWRON_I2_MAXBUS  10B4> 19B5<
=PP3V3_PWRON_I2_MISC  10B5< 22B6< 22C7<
=PP3V3_PWRON_INVERTER  10B4> 56B4<
=PP3V3_PWRON_JTAG_ASIC  9C8< 10B5<
=PP3V3_PWRON_LCD  10B4> 56C8<>
=PP3V3_PWRON_LEFT_ALS  7B5> 10B4> 31C3<>
=PP3V3_PWRON_LTC3412  10B4> 17D6<
=PP3V3_PWRON_MMM  10B4> 29C6<
=PP3V3_PWRON_MODEM  10B4> 30B4<>
=PP3V3_PWRON_PMU  10B4> 25B8<
=PP3V3_PWRON_REG  10B6<> 15D1<
=PP3V3_PWRON_RT_ALS  10B5< 28D5<
=PP3V3_PWRON_RUNFET  10B4> 15B2<>
=PP3V3_PWRON_TPS2211  10B4> 61D4<
=PP3V3_PWRON_USB2  10A4> 73B6< 73C6< 73D5<
=PP3V3_PWRON_VDDSPD  10B5< 40A6<> 41A4<> 41A6<>
=PP3V3_PWRON_VGASYNC  10B4> 57C2< 57C2<
=PP3V3_RUN_AUDIO  7A7> 10B3< 74B3<>
=PP3V3_RUN_FANTACH  10B1> 27D2<
=PP3V3_RUN_FWPORTPWRSW  10B1> 18C8<
=PP3V3_RUN_HDD   10B1> 64B8< 64C7<
=PP3V3_RUN_KEYBRD_LED  10B1> 28B6<
=PP3V3_RUN_PCI1510_R  10B1> 61D7<
=PP3V3_RUN_PWRSEQ  10B3< 26B7< 26C6<
=PP3V3_RUN_RUNFET  10B3< 15B1<>
=PP3V3_RUN_SI     10B1> 54C2< 54C3< 54C5< 55C3<
            55D3< 55D3<
=PP3V3_VESTA      10D4> 18A2< 18A6< 18A8< 66C7<
=PP3V3_VESTA_1V2REG  10D4> 18C5<
=PP3V3_VESTA_2V5REG  10D4> 18D3<
=PP3V3_VESTA_REG  10D6< 18D3<
=PP4V85_ALL_A29_DET  10C6> 12D4<
=PP4V85_ALL_VREG  10C8< 14B4<>
=PP5V_FAN1_PWR   7C5> 10C1> 31B4<>
=PP5V_FAN2_PWR   7C5> 10C1> 31B3<>
=PP5V_PWRON_AUDIO_AVDD  10C4> 74C7<>
=PP5V_PWRON_AUDIO_PVDD  10C4> 74C7<>
=PP5V_PWRON_CPUVCORE_PWRSEQ  10C3> 36C8<
=PP5V_PWRON_CPUVCORE_VDD  10C4> 36C6<>
=PP5V_PWRON_GPUVCORE_PWRMSR  10C3> 45B5<
=PP5V_PWRON_INVERTER  10B4> 56C4<>
=PP5V_PWRON_LEFT_USB  7B5> 10C4> 31B3<>
=PP5V_PWRON_LTC1625_EXTVCC  10C4> 14D7<>
=PP5V_PWRON_LTC1778_GPU_EXTVCC  10C3> 45D6<
=PP5V_PWRON_LTC3707_EXTVCC  10C4> 15D5<
=PP5V_PWRON_MAX1715_VDD  10C4> 16D5<>
=PP5V_PWRON_PMU_SUPPLY  10C4> 14B4<>
=PP5V_PWRON_PWRSEQ  10C4> 26C7< 26D7<
=PP5V_PWRON_REG  10C6<> 15D8<
=PP5V_PWRON_RIGHT_USB  7B5> 10C4> 31B7<>
=PP5V_PWRON_RUNFET  10C4> 15B5<>
=PP5V_PWRON_SLEEPLED  10B4> 24B7<
=PP5V_PWRON_TPS2211  10C4> 61D4<
=PP5V_PWRON_TRACKPAD  10B4> 15B8<>
=PP5V_RUN_DVI_DDC  10C1> 57D4<
=PP5V_RUN_FANPWM  10C1> 27D2<
=PP5V_RUN_HDD    7B7> 10C1> 64B5<> 64B8<
=PP5V_RUN_HDDFET  10C3< 15B4<>
=PP5V_RUN_KEYBRD_LED  10C1> 28B5<
=PP5V_RUN_ODD    7B7> 10C1> 64C4<
=PP5V_RUN_PWRSEQ  10C1> 26A7< 26C8<
=PP5V_RUN_RUNFET  10C3< 15A4<>
=PP5V_SUPERCAP   14A4< 31A6<
=PP5V_TPAD        10C1> 30D6<
=PP5V_TPAD_FET   10C3< 15A6<>
=PP12V8_LTC1625_VREG  10D8< 14C3<>
=PP12V8_PBUSB_HOLDUP_CAPS  10D6> 31D3<
=PP12V8_PBUS_PMU_SUPPLY  10D6> 14A7<>
=PP14VR24V_ALL_PBUS_A  10D8> 13D5<
=PP24V_ADAPTER_CONN  10C8< 31D7<>
=PP24V_ADAPTER_PMU_SUPPLY  10C6> 14A7<
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=PPBUS_INVERTER  10D6> 56C3<
=PPBU_RUN_FW     10C1> 18D6<>
=PPFW_P3V3VESTA  10D4> 18D6<>
=PPFW_PHY_CPS    10D4> 69C5<
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=PPI2C_GPU       8B5< 10B1>
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=PPI2C_I2_SB     8D2< 10B5<
=PPI2C_SYS0      8B5< 10C6>
=PPI2C_SYS1      8C5< 10B5<
=PPJTAG_CPU      9D8< 10A1>
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=PPVBATT_BATTERY_PMU_SUPPLY  10C6> 14A7<
=PPVBATT_BATT_PBUSA  10D8< 13D2<>
=PPVBATT_BATT_PBUSB  10D8< 13D1<>
=PPVBATT_BATT_VSNS  10C8< 12B6<
=PPVBATT_ISNS_N  10C8< 12B4<>
=PPVCORE_CPU0    10C4> 35C4< 35C8< 35D4<
=PPVCORE_CPU_ADT7467  10C4> 27C4<
=PPVCORE_CPU_REG  10C6< 36C1<
=PPVCORE_GPU_REG  10A8<> 45C3<>
=PPVCORE_PWRON_I2  10A6> 19D6<
=PPVCORE_PWRON_I2_REG  10A8<> 20C2<
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=PPVIN_ALL_LTC1625  10D6> 14D3<>
=PPVIN_ALL_LTC3707  10D6> 15D5<>
=PPVIN_ALL_MAX1715  10D6> 16C3<> 16C7<> 16D5<
=PPVIN_BATT_CHRG_VSNS  10C6> 13A4<
=PPVIN_CPU0_AVDD  10B3> 37C7<
=PPVIN_CPUVCORE_MAX1717  10D6> 36D4<>
=PPVIN_GPU_LVDDR_LDO  10B6> 52B4<
=PPVIN_LTC1778_GPU  10D6> 45D5<>
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=SLEEP_LED_CONN  11A3> 74B3<>
=SLEEP_LED_IOUT  11A5< 24B6<
=SPI_I2_CLK      22A5<
=SPI_I2_MISO     22B2>
=SPI_I2_MOSI     22B5<
=SPI_I2_REQ      11A5< 22A7< 22C5<
=SYSCLK_TBEN_SYNC  11D4> 21A5< 21D6>
=TPS2211_SHDN_L  10B3< 61D5<
=VCORE_PGOOD     26B5< 36B4>
=VESTA_CLK25M_TX  11A6> 66C2>
=VESTA_CLK125M_GBE_REF  11A6> 66C2>
=VESTA_CLK125M_RX  11A6> 66C2>
=VESTA_ENERGYDET  11A6> 66B3>
=VESTA_MDC       11A6> 66B6<>
=VESTA_MDIO      11A6> 66B6<>
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A29_CURRENT_ADJ  13C4<>
A29_DETECT       12D1< 13A5<> 13C4<>
A29_DET_L        12C2<
A29_DET_REF      12C2<
AB_SEL_LOW       36A6<>
AC_DET_DIV       12C7<
AC_ENABLE_GATE   12D5<>
AC_ENABLE_L      12C5<>
AC_GTR_18V       13C3<>

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ADT7467_ADR_ENABLE_L  27C2<>
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AGP_AD<31>       43B3< 44B6<>
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AGP_AD_STB0_P    43B2< 43C3< 43D6> 44B4<>
AGP_AD_STB1_N    43A2< 43B3< 43D6> 44B4<>
AGP_AD_STB1_P    43B2< 43B3< 43D6> 44B4<>
AGP_ATI_RESET_L  44C4<
AGP_BUSY_L       43D2< 43D5< 44B4>
AGP_CBE_L<0>     43C3< 44C4<>
AGP_CBE_L<1..0>  43D6>
AGP_CBE_L<1>     43C3< 44C4<>
AGP_CBE_L<2>     43B3< 44C4<>
AGP_CBE_L<3..2>  43D6>
AGP_CBE_L<3>     43B3< 44C4<>
AGP_CLK66M_GPU   11C7< 44C4< 44D6>
AGP_CLK66M_GPU_R  11C8< 43D3< 43D6>
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AGP_FRAME_L      6B6< 43D5< 43D6> 44C4<>
AGP_GNT_L        6B6< 43C6> 43D3< 44C4<
AGP_INT_L        22D5< 43C2< 44C4>
AGP_IRDY_L       6B6< 43C5< 43C6> 44C4<>
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AGP_PIPE_L       43B2< 43C5< 43C6>
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AGP_REQ_L        6B6< 43C6> 43D5< 44C4<>
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AGP_SBA<6>       43C5< 44B6>
AGP_SBA<7>       43C5< 44B6>
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AGP_TRDY_L       6B6< 43C5< 43C6> 44C4<>
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AIRPORT_CLKRUN_L_PD  60C4<>
ALS_0_OUT        7B5> 25A6> 31C4<>
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ANALOG_AC_DET    12C3<
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ATI_CLK27M_SS_R  52A6<> 52D6>
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ATI_RSET         53B6<
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AUDIO_CODEC_RESET_L  7A7> 22C5< 74B3<>
AUDIO_EXT_MCLK_SEL  7A7> 22C5< 74B4<>
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AUDIO_I2S_DTIB_SEL  7A7> 22C5< 74B4<>
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AUDIO_LI_OPTICAL_PLUG_L  7A7> 22D5< 74B4<>
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AUDIO_LO_MUTE_L  7A7> 22C5< 74B4<>
AUDIO_LO_OPTICAL_PLUG_L  7A7> 22C5< 74B4<>
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AUDIO_SPDIF_RXERR_INT  74B4<>
AUDIO_SPKR_MUTE_L  7A7> 22C5< 74B4<>
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BATTV_LOW        13B8<>
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BATT_14V_GATE    13C1<>
BATT_24PBUS_EN   13C2<>
BATT_24V_GATE    13C1<>
BATT_CLK         12A7<>
BATT_DATA        12A7<>
BATT_DIV         13A5<
BATT_ISNS        12A3< 25A3>
BATT_ISNS_R      12A4<>
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FWPWR_ACIN       18B7<>
FWPWR_EN         18C7<>
FWPWR_EN_L       18C7<
FWPWR_EN_L_DIV   18C7<>
FWPWR_PWRON      26D4<
FWPWR_RUN        18C7<>
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FW_CLK98M_PCLK   68C5< 68D6> 69C1>
FW_CLK98M_PCLK_R  69C3<> 69D6>
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FW_PORT1_TPA_P   70C5<> 70C5>
FW_PORT1_TPA_P_FL  70C2<> 70D6>
FW_PORT1_TPB_N   70C5> 70D5<>
FW_PORT1_TPB_N_FL  70D2<> 70D6>
FW_PORT1_TPB_P   70C5> 70D5<>
FW_PORT1_TPB_P_FL  70D2<> 70D6>
FW_PORT2_TPA_N   70A5<> 70C5>
FW_PORT2_TPA_N_FL  70A3<> 70D6>
FW_PORT2_TPA_P   70B5<> 70C5>
FW_PORT2_TPA_P_FL  70A3<> 70D6>
FW_PORT2_TPB_N   70A5<> 70C5>
FW_PORT2_TPB_N_FL  70A3<> 70D6>
FW_PORT2_TPB_P   70A5<> 70C5>
FW_PORT2_TPB_P_FL  70A3<> 70D6>
FW_POWERDOWN     22A7< 22C5<
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FW_TPA0_N        69B2<> 69D6> 70C7<
FW_TPA0_P        69B2<> 69D6> 70C7<
FW_TPA1_C        70C6<
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FW_TPA1_P        69B2<> 69D6> 70C7<
FW_TPA2_N        69B2<> 69D6> 70B7<
FW_TPA2_P        69B2<> 69D6> 70B7<
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FW_TPB0_P        69B2<> 69D6> 70C7<
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GND_INVERTER     7B7> 56B2<>
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GND_PMU_AVSS     25A3<> 25D3< 28D3< 29B3< 31B4<
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GPUVCORE_SHDN_L  26B6< 45C7<
GPUVDD15_EN      26A5< 46B5<>
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GPU_DVO_VSYNC    6C3> 54A6< 54C6> 55A6< 55D6>
GPU_DVO_VSYNC_R  6C4< 53C7<> 53D1>
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GPU_MEMVMODE0    48A6<
GPU_MEMVMODE1    48A6<
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GPU_MVREFS       48A8<
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GPU_SSIN_PD      51B4<
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GPU_VCORE_HI_L_RC  45A5<>
GPU_VCORE_SW     45C4<>
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HIGH_GPU_VCORE_L  45B3<>
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HPD_ON_RC        57A3<
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I2C_GPU_TMDS_SDA  8A5< 8D6>
I2C_I2_NB_SCL    8C2< 8D6>
I2C_I2_NB_SDA    8C2< 8D6>
I2C_I2_SB_SCL    8D2< 8D6>
I2C_I2_SB_SDA    8D2< 8D6>
I2C_PMU_SCL      8C5< 8D6>
I2C_PMU_SDA      8C5< 8D6>
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I2C_PMU_SMB_SDA  8B5< 8D6>
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I2C_VESTA_SDA  69B3<>
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I2S0_BITCLK_R  6D8< 22B2< 22D6>
I2S0_DEV_TO_SB_DTI  7A7> 22B5< 22D6> 74C4<>
I2S0_MCLK  6D6> 7A7> 74B3<>
I2S0_MCLK_R  6D8< 22B2< 22D6>
I2S0_SB_TO_DEV_DTO  6D6> 7A7> 74B4<>
I2S0_SB_TO_DEV_DTO_R  6D8< 22B2< 22D6>
I2S0_SYNC  6D6> 7A7> 74B3<>
I2S0_SYNC_R  6D8< 22B2< 22D6>
I2S1_BITCLK  6D6> 30A5<>
I2S1_BITCLK_R  6D8< 22B2< 22D6>
I2S1_DEV_TO_SB_DTI  22B5< 22D6> 30A5<>
I2S1_MCLK  6D6> 30A4<>
I2S1_MCLK_R  6D8< 22B2< 22D6>
I2S1_SB_TO_DEV_DTO  6D6> 30A5<>
I2S1_SB_TO_DEV_DTO_R  6D8< 22B2< 22D6>
I2S1_SYNC  6D6> 30A5<>
I2S1_SYNC_R  6D8< 22B2< 22D6>
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I2VCORE_ITH_RC  20C6<
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I2VCORE_MODE_VDIV  20C5<
I2VCORE_RT  20C5<
I2VCORE_RUNSS  20C5<>
I2VCORE_SW  20C4<>
I2VCORE_VFB  20C5<>
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I2_AGP_FBCLK_OUT  21C5< 43A2< 43D6>
I2_AGP_FBCLK_OUT_R  43A3< 43D6>
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I2_CLK18M_XOUT  22A6< 22D6>
I2_CLK18M_XOUT_R  22A5< 22D6>
I2_CLK30M_USB2_XIN  72B6< 72D6>
I2_CLK30M_USB2_XOUT  72B7< 72D6>
I2_CLK30M_USB2_XOUT_R  72B6< 72D6>
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I2_EXT_13  22C5<
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I2_FW_PVT  68C5<
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I2_GPIO_EXT_02  11A5< 22A7< 22C5<
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I2_MAXBUS_FBCLK_MATCHED  21D4< 21D6>
I2_MAXBUS_FBCLK_OUT  21D6< 32A2< 32D6>
I2_MAXBUS_FBCLK_OUT_R  32A4< 32D6>
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I2_PCI_FBCLK_OUT_R  59A4< 59D6>
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I2_TST_TEI  22B5<
I2_UATA_VREF  63B5<
I2_USB2_VREF  72B5<
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IAC_RC_COMP  13D4<
INV_ON_PWM  53B8<> 56B4<
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JTAG_ASIC_TMS  9B8<
JTAG_ASIC_TRST_L  9B8<
JTAG_CPU_TCK  9D7<
JTAG_CPU_TDI  9D7<
JTAG_CPU_TMS  9D7<
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JTAG_I2_TDI  9C7<
JTAG_VESTA_TRST_L  9A8<
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KBDLED_RETURN  7C5< 28A4< 30C6<>
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LCD_PWREN_L  56C7<>
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LTC3412_GND  17B5<>
LTC3412_ITH  17C5<>
LTC3412_ITH_RC  17C6<
LTC3412_RT  17C5<>
LTC3412_RUNSS  17C5<>
LTC3412_SW  17C4<>
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MAX1715_SKIP  16C4<
MAX1715_TON  16C5<
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MAX8860_FAULT_L  52B3<>
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MAXBUS_CPU0_QACK_L  32D3< 33B1<
MAXBUS_CPU0_QREQ_L  32B2< 32D5< 33C1<
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SIZE	DRAWING NUMBER	REV.
D	051-6839	02
SCALE NONE	SHT 113	OF 115

*** Part Cross-Reference for the entire design ***

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U1200	COMPARATOR_LMC7211	12
U1220	COMPARATOR_LMC7211	12
U1250	INA138	12
U1300	MAX1772	13
U1350	COMPARATOR_LMC7211	13
U1370	AMP_MAX4172	13
U1380	OPAMP_LMC7111	13
U1400	LTC1625	14
U1420	COMPARATOR_LMC7211	14
U1450	VREG_LP2951	14
U1460	VREG_LP2951	14
U1500	LTC3707	15
U1600	MAX1715	16
U1700	LTC3412	17
U1970	VREG_LM2594	18
U1980	VREG_MM1572FM	18
U1990	LTC3411	18
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U2250	VREG_LT1962	20
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U2391	SN74AUC1G74	21
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U2500	CLK_DR_CDCVF2505	23
U2700	M38280M8	25
U3000	ADT7467	27
U3100	OPAMP_MAX4236EUTT	28
U3130	MM3120	28
U3220	KXMS2	29
U3600	A8	33 34 35
U3900	MAX1717	36
U3990	PI3B3257	36
U4600	FAN2558	37
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U5800	LTC1778	45
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U6530	MAX8860	52
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U6800	SIL1178CS48	55
U6953	NC7S32	56
U7050	74LG32	57
U7051	74LG32	57
U7070	COMPARATOR_LMC7211	57
U7100	FEPR_1MX8	58
U7400	PCI1510GGU	61
U7450	PWR_CNTRL_TPS2211	61
U7500	UPD720101_FBGA_SPLIT	62 73
U8500	BCM5462	18 66 69
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Y2750	CRYSTAL	25
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Y9220	CRYSTAL	72
Y9345	CRYSTAL	73
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ZT0230	MTGHOLE	2
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ZT0257	HOLE_VIA	2